Hitachi Power Mos Fets

Lateral Gate and Vertical Gate types
Data Sheets
Applications Information

Note) The specification of these devices are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of a semiconductor-applied product.
The Company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

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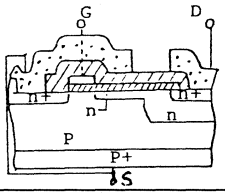
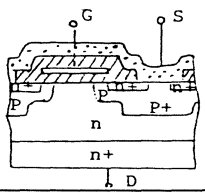
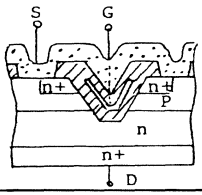
PRODUCT SELECTION D Series or S Series?

Power MOS FETs are used in communications and many industrial applications such as high-speed high-power switches, high-frequency power amplifiers and ultrasonic generators. The characteristics which make them so ideal are (1) high switching speed, (2) good frequency characteristics, and (3) a wide area of safe operation. In addition to the conventional 2SK259 H (V_{DSS} = 350V) and 2SK260 H (V_{DSS} = 400V) devices of the high-power-rating series (S series), HITACHI is now marketing the D series. For example 2SK298 H (V_{DSS} = 400V) and 2SK299 H (V_{DSS} = 450V) devices of this higher-power-rating low-on-resistance series to meet wider needs.

• Construction and Electrode

As shown in Table 1, the S series has the source, channel and drain paralleled horizontally, so that the drain current flows horizontally. The substrate and source are at the same potential, and the case serves as the source electrode. In the D series, by contrast, the source, channel and drain are disposed vertically, so that the drain current flows vertically. With the substrate constituting the drain, the case then serves as the drain electrode.

Type		S. Series Offset Gate	D. Series Vertical Type	V Type
Device Structure				
Typical Features	V_{DS}	Fair	Good	Fair
	R(on)	Fair 2.5Ωtyp.	Low 1.0Ω typ.	Good
	Complementry	Good	Poor	Fair
	A.S.O	Very large (approximately twice larger than that of the D series.)	Larger than that of bipolar transistors even in the high-pressure area.	Fair
	Terminal	Source Case	Drain Case	Drain Case
	Switching Speed	Fair	Fair	Good
	Gate Protection	Good	Poor	Good

• On-resistance

As shown in Fig. 1, on-resistance of the D series is as low as 1.0Ω, as compared with the relatively high 2.5Ω values for the S series.

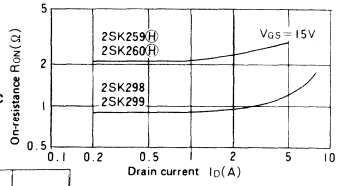


Fig. 1 On-resistance vs. drain current characteristic

• A.S.O. (Area of Safe Operation)

Due to the lack of the secondary breakdown area exhibited by bipolar transistors the A.S.O. of power MOS FETs can be guaranteed in terms of an equipotential line even in the high-voltage area. In the A.S.O. under 10-second power application, the S series exhibit a maximum channel power dissipation of approximately 400W and a maximum channel voltage of 400V. The maximum channel power dissipation of the D series is approximately 200W, as shown in Fig. 2.

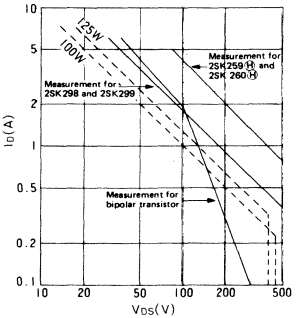


Fig. 2 DC A.S.O. (Area of Safety Operation)

- **Frequency Characteristic and Switching Speed**

As shown in Fig. 3, the cut-off frequency ranges between 5 and 8MHz for both the S and the D series. Standard switching times are as follows: t_{on} = 25ns and t_{off} = 140ns for the S series: t_{on} = 25ns and t_{off} = 180ns for the D Series.

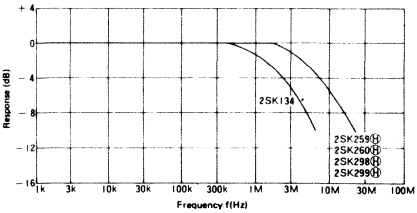


Fig. 3 Frequency characteristic of amplification factor

- **Gate Protection**

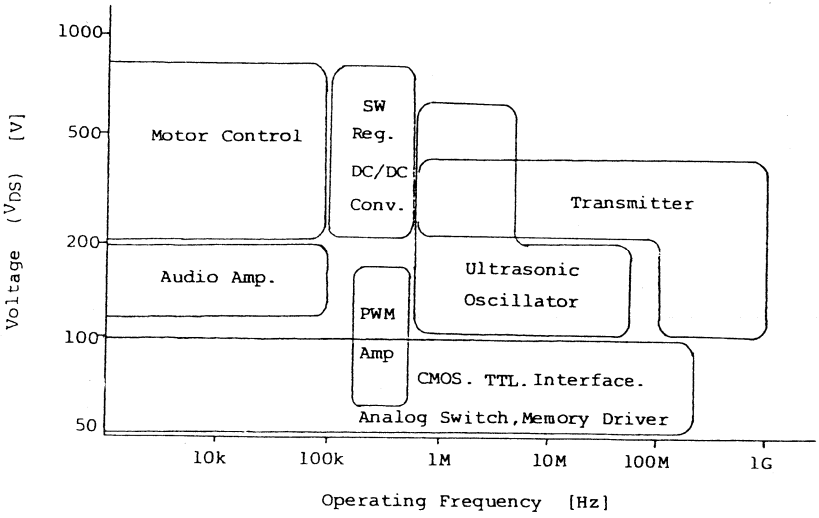
As shown in Table 1, the S series has a protection diode between the gate and source to provide protection against electrostatic breakdown. Having no such diode, the D series requires care in handling. Do not touch the gate electrode. Also, devices, working tables and process operators must be properly grounded

- **Parallel Operation**

Both S and D series can be paralleled to increase their capacity. Because of this, they are suited for high-speed large-capacity switching regulators, high-efficiency high-frequency amplifiers, ultrasonic wave oscillators, PWM amplifiers, solenoid and motor driving circuits, and many other applications.

- **Application Map**

Further details in the applications section give typical circuits and example PCB layouts etc.



Main Characteristics

D SERIES

Type No.		Maximum Ratings				Electrical Characteristics					Outline
N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}** (W)	R_{on} (Ω) typ	R_{on} (Ω) max	t_{on} (ns)	t_{off} (ns)	f_c (MHz)	
2SK352	–	250	±15	0.3	10	30	–	–	–	–	T-126
2SK347	–	400	±20	1	10	3.0	5.0	–	–	–	T-24
2SK294	–	80	±20	5	30	0.4	0.56	40	70	5	T-220AB
2SK295	–	100									
2SK296	–	300		1		2.5	4.0	20	70	10	
2SK310	–	400		3	50	2.5	4.0	25	70	10	
2SK311	–	450									
2SK319	–	400		5		1.1	1.83	50	120	5	
2SK320	–	450									
2SK343	2SJ99	140	±20	8	100	0.4	0.5	100	90	–	T-22
2SK344	2SJ100	160									
2SK345	2SJ101	40		5	30	0.3	0.4	30	40	–	T-220
2SK346	2SJ102	60									
2SK308	–	120	±20	10	100	0.2	0.3	60	160	4	T-3
2SK298	–	400		8	100	1.1	1.75	50	120	5	
2SK299	–	450									
2SK312	–	400		12	125	0.67	0.9	70	200	3	
2SK313	–	450									
2SK351	–	800		5	125	1.7	3.0	100	300	2	

** T_C = 25 °C ( ) Under development

Type No.		Maximum Ratings				Electrical Characteristics					Outline
N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}** (W)	R_{on} (Ω) typ	R_{on} (Ω) max	t_{on} (ns)	t_{off} (ns)	f_c (MHz)	
2SK213	2SJ76	*140	±15	0.5	30	8/10	–	20	30	40/30	T-220AB
2SK214	2SJ77	*160									
2SK214Ⓚ	2SJ77Ⓚ	160									
2SK215	2SJ78	*180									
2SK216	2SJ79	*200									
2SK216Ⓚ	2SJ79Ⓚ	200									
2SK196Ⓗ	–	160	±15	0.5	0.8	8	–	20	30	30	T-39
2SK286	2SJ96	* 60	±20	8	100	0.5	0.8	80/100	110/250	3/2	T-22
2SK287Ⓚ	–	60				0.5	0.6	25	350	2	
2SK288Ⓚ	–	80									
2SK225	2SJ81	*120	±15	7		1.0	1.7	180/230	60/110	3/2	
2SK226	2SJ82	*140									
2SK227	2SJ83	*160									
2SK133	2SJ48	*120	±14	7	100	1.0	1.7	180/230	60/110	3/2	T-3
2SK134	2SJ49	*140									
2SK134Ⓗ	2SJ49Ⓗ							90/150	110/210		
2SK135	2SJ50	*160						180/230	60/110		
2SK135Ⓗ	2SJ50Ⓗ							90/150	110/210		
2SK175	2SJ55	*180	±20	8	125	1.0	1.7	270/330	90/120	2/1	
2SK176	2SJ56	*200									
2SK176Ⓗ	2SJ56Ⓗ	200						60	200		
2SK220Ⓗ	–	160	±20	8	100	1.0	1.5	25	45	50	
2SK221Ⓗ	–	200									
2SK258Ⓗ	–	250		8	125	0.8	1.1	25	140	7	
2SK259Ⓗ	–	350		5	125	2.5	3.0	25	140	7	
2SK260Ⓗ	–	400									
2SK317	–	180	±20	8	120	0.95	1.25	–	–	300	T-40
2SK318	–			4	70	1.9	2.5				

* V_{DSX} ** T_C = 25 °C

Handling Precautions

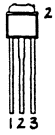
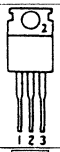
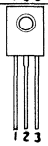
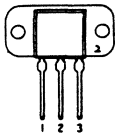
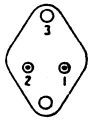
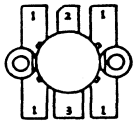
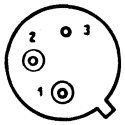
Handling precautions and simple checking methods will be described for the benefit of those who use Hitachi's power MOS FETs.

If handled improperly, power MOS FETs cannot display their excellent performance described in the foregoing. Not only that. Improper use can lead to destruction of the devices.

Also, it is necessary to take into consideration the abnormal oscillation due to high gain, high input impedance, and excellent high frequency characteristics, which are some of the features of power MOS FETs.

By observing these precautions, circuits can be designed with outstanding performance that cannot be expected from using conventional power devices.

Pin Arrangement

	Package	Lead configration					
		D Series			S Series		
		1	2	3	1	2	3
DPAK		Gate	Drain	Source	–	–	–
TO-220 AB		Gate	Drain (Flange)	Source	Gate	Source (Flange)	Drain
TO-126 mod.		Source	Drain	Gate	–	–	–
HPAK		Gate	Drain (Flange)	Source	Gate	Source (Flange)	Drain
TO-3		Gate	Source	Drain (Case)	Gate	Drain	Source (Case)
RFPAK		–	–	–	Source	Drain	Gate
TO-39		–	–	–	Drain	Gate	Source (Case)

*1 Ta ≦ 30C, RH= 20～80% PC is a condition which is assumed as less than 60% of rating

	SUFFIX	(H)	(K)	NO SUFFIX
FIELD FAILURE RATE *1	Resin moulded type small signal FET	-	10	25
	Hermetic sealed type small signal FET	5	-	25
	Resin moulded type Power FET	-	30	50
	Hermetic Sealed type Power FET	20	-	50
MANUFACTURING PROCESS	Visual Inspection	100% Inspection ↓ Lot Acceptance Inspection AQL = 0.25%	Lot Acceptance Inspection AQL = 0.25%	LOT LEVEL ACCEPTANCE (MACHINE BY MACHINE)
FINAL INSPECTION	Static Characeristics Visual severe failure	AQL = 0.065%	AQL = 0.065%	AQL = 0.1%
	Static slight failure	0.25	0.4	1.0
	Operating Characteristics	0.65	1.0	1.0
	Visual slight failure	0.65	1.0	2.5
RELIABILITY TEST	Lot Acceptance Test	GV 1: Visual, dimension, solderability — LTPD 15% GV 2: Soldering Heat Temperature Cycle, Thermal Shock, High Humidity — LTPD 15% GV 3: Mechanical Shock Vibration Variable Frequency, Constant Acceleration — LTPD 15% GV 4: Lead Intensity — LTPD 15% GV 5: Pressure Cooker — LTPD λ=10 GV 6: Operational rating lif test — LTPD λ=10	High Humidity (PCT = 24 hr)	No Test
	Regular Reliability Test	1 Life Test 2 Thermal stress Test 3 Mechanical Stress Test 4 General Circumstance Test	The same as the left	The same as the left

TO18, TO72, TO39, MPAK, FPAK, TO92, TO92M, TO3, (TO66), HPAK, TO220, TO202, TO126, DPAK etc

Beside the standard process a high reliability telecommunicaiton inspection procedure is available to special request.

Reliability

High quality and high reliability are achieved in power MOS FETs by applying the process technology and quality control established for MOS LSI and bipolar power transistors.

In order that you may use Hitachi's power MOS FETs with high reliability, explanation will be given by referring to reliability test data.

(1) Reliability design and process features

The chip structure of a power MOS FET is illustrated in Fig. 5. In order to achieve high voltage durability and high output characteristics, the following design and process considerations are given:

- **Chip structure**

To ease electric field concentration between source and drain, a low-concentration dopant is implanted by ion implantation, to form an offset gate structure. Further, by providing a source field plate, high voltage durability is achieved.

- **Chip fabrication process**

Since micropatterns and integration degrees similar to those of LSI are used, basic process technologies established for MOS LSI, such as surface passivation and electrode formation, are applied.

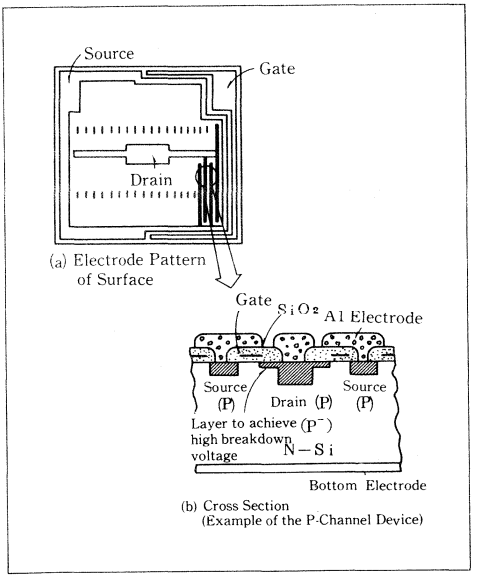


Fig. 5 Pattern of Surface and Cross Section of Power MOS FET

Reliability data

- **Failure criteria**

Items for reliability tests and failure criteria are presented in Table 1.

Table 2 Failure Criteria

Item	Symbol	Failure Criteria (Note)		Unit
		Lower	Upper	
Breakdown Voltage	$V_{(BR)DSX}$ $\pm V_{(BR)GSS}$	L x 0.8	–	V
Leak Current	I_{DSX} $\pm I_{GSS}$	–	U x 2	μA
Cut-off Voltage	$V_{GS\ (off)}$	0	U x 1.2	V
Saturation Voltage	$V_{DS\ (sat)}$	–	U x 1.2	V
Saturation Voltage Ratio	$\triangle V_{DS\ (sat)}$	−30	+ 30	%
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	L x 0.8	U x 1.2	S
Forward Transfer Admittance Ratio	$\triangle \lvert y_{fs} \rvert$	− 30	+ 30	%

(Note) U: Upper Limit After the Test
L: Lower Limit After the Test

RELIABILITY TEST RESULTS

The results of reliability tests on complementary pair power MOS FETs 2SK135/2SJ50 are given in Table 3

Table 4 shows the temporal changes of major parameters in device life tests.

Table 3 Test Results

Item	Test Conditions	N-Channel (2SK135)			P-Channel (2SJ50)		
		Sample Number (pcs)	Testing Time (hr)	Failure (pcs)	Sample Number (pcs)	Testing Time (hr)	Failure (pcs)
Operating Life Test	Ta=25°C, Pch=27W, V_{DS}=80V Heat Sink θ_f=3°C/W (T_j=150°C)	80	2,000	0	100	2,000	0
High Temperature Reverse Bias Test	Ta=150°C, V_{DSX}=160V, V_{GS}=−10V	125	2,000	0	140	2,000	0
Humidity Test	Ta=80°C, RH≧90%	77	2,000	0	77	2,000	0
Low Temperature Storage Test	Ta=−55°C	45	2,000	0	45	2,000	0
Thermal Fatigue Test	ΔT_C=90°C, Tjmax=150°C ON: 1 minute, OFF: 1.5 minutes	50	10k cycles	0	50	10k cycles	0
Temperature Cycle Test	−55~+150°C, 30 minutes each	730	10 cycles	0	580	10 cycles	0
Resistance to Soldering Heat Test	260°C, 10 seconds	22	–	0	22	–	0
Drop Shock Test	1500G, 0.5ms, XYZ(3 times each)	77	–	0	77	–	0
Vibration Fatigue Test	60Hz, 20G, XYZ(32 hours each)	38	–	0	38	–	0
Vibration-Variable Frequency Test	100~2000Hz, 20G, cycle time 4 min. XYZ (3 times each)	38	–	0	38	–	0
Constant Acceleration Test	20000G, XYZ(1 minute each)	38	–	0	38	–	0
Capability Against Electrostatic Discharge Test	C=200pF, V=300V forward and reverse polarity between G-S (one time each)	100	–	0	100	–	0

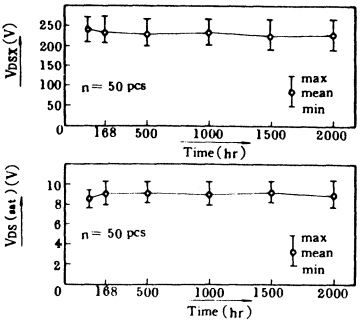
Table 4 Changes of Major Parameters

Type No.	2SK135
Test item	High temperature reverse bias test
Test condition	Ta = 150°C V_{DSX} = 160V, V_{GS} = −10V
Failure criteria	V_{DSX} = higher then 128V $V_{DS(sat)}$ = lower then 1.4V $\Delta V_{DS(sat)}$ = within ± 80%
Failure mode	Surface degradation

Description

1. There is almost no breakdown voltage change after 2,000 hours.
2. Change of $V_{DS(sat)}$ increases a little at the initial period, but the changes is completely saturated after 2,000 hours.
3. There is almost no degradation of V_{GSS} I_{DSS} and other parametes.

Changes of breakdown voltage and saturation voltage



2SJ48/49/50
(COMPLEMENT TO 2SK133/134/135)

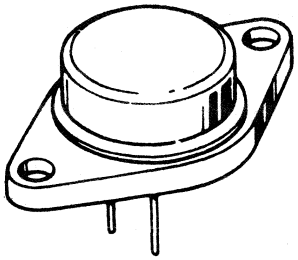
SILICON P CHANNEL MOS FET

LOW FREQUENCY POWER AMPLIFIER

Complementary Pair with 2SK133, 2SK134
2SK135

Features;

1. High Power Gain.
2. Excellent Frequency Response.
3. High Speed Switching.
4. Wide Area of Safe Operation.
5. Enhancement-mode.
6. Good Complementary Characteristics.
7. Equipped with Gate Protection Diodes.



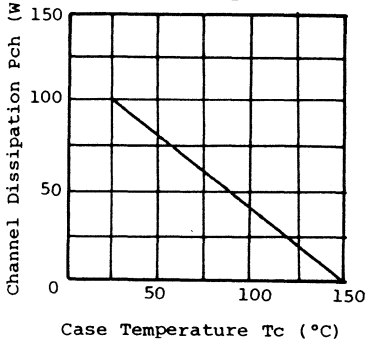
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating			Unit
		2SJ48	2SJ49	2SJ50	
Drain to Source Voltage	V_{DSX}	-120	-140	-160	V
Gate to Source Voltage	V_{GSS}	±14	±14	±14	V
Drain Current	I_D	-7	-7	-7	A
Channel Dissipation	Pch*	100	100	100	W
Channel Temperature	Tch	150	150	150	°C
Storage Temperature	Tstg	-55 ~ +150	-55 ~ +150	-55 ~ +150	°C

*Value at Tc=25°C

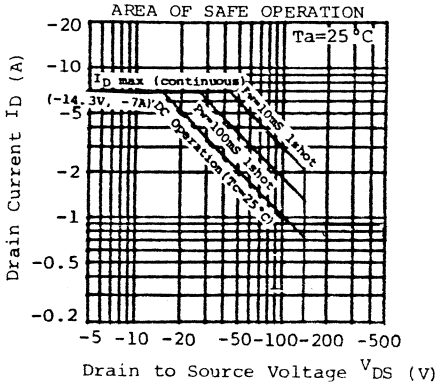
MAXIMUM CHANNEL DISSIPATION CURVE



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	2SJ48			2SJ49			2SJ50			Unit
			min	typ	max	min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	I_D=-10mA, V_{GS}=10V	-120	–	–	-140	–	–	-160	–	–	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±14	–	–	±14	–	–	±14	–	–	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=-100mA, V_{DS}=-10V	-0.15	–	-1.45	-0.15	–	-1.45	-0.15	–	-1.45	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=-7A, V_{GD}=0 *	–	–	-12	–	–	-12	–	–	-12	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-10V, I_D=-3A *	0.7	1.0	1.4	0.7	1.0	1.4	0.7	1.0	1.4	S
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=-10V f=1MHz	–	900	–	–	900	–	–	900	–	pF
Output Capacitance	Coss		–	400	–	–	400	–	–	400	–	pF
Reverce Transfer Capacitance	Crss		–	40	–	–	40	–	–	40	–	pF
Turn on Time	t_{on}	V_{DD}=-20V, I_D=-4A	–	230	–	–	230	–	–	230	–	ns
Turn off Time	t_{off}		–	110	–	–	110	–	–	110	–	ns

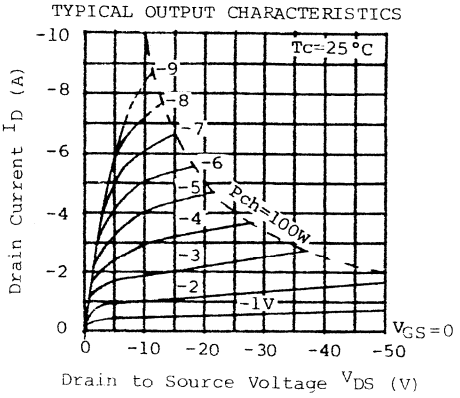
*Pulse Test

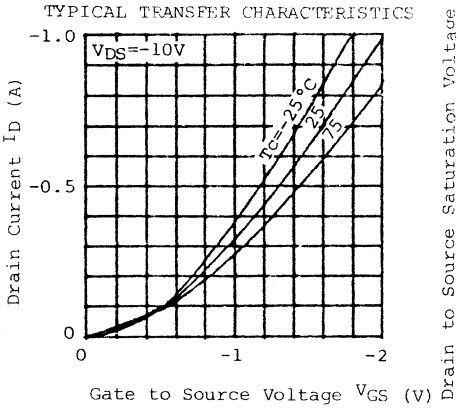


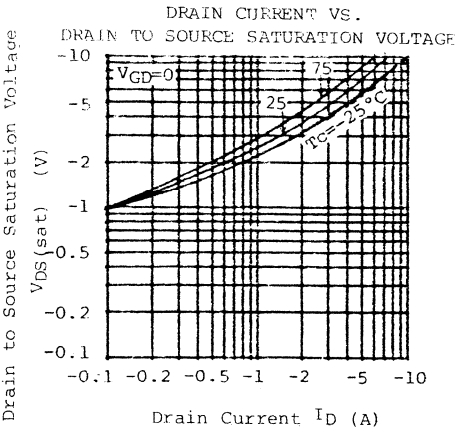
ASO LEVELS DC OPERATION AND ONE-SHOT ABILITY

DC operation levels
2SJ48 -120V -0.83A
2SJ49 -140V -0.71A
2SJ50 -160V -0.63A

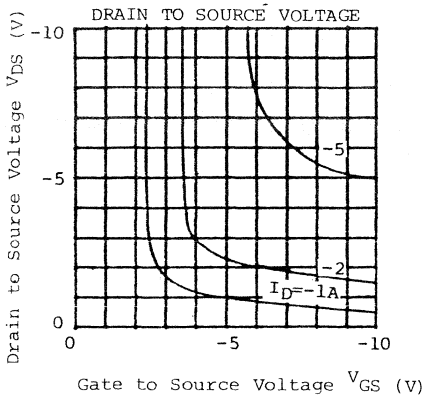
GENERAL CHARACTERISTICS ALL DEVICES



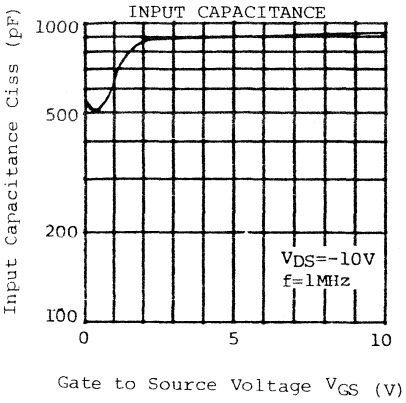




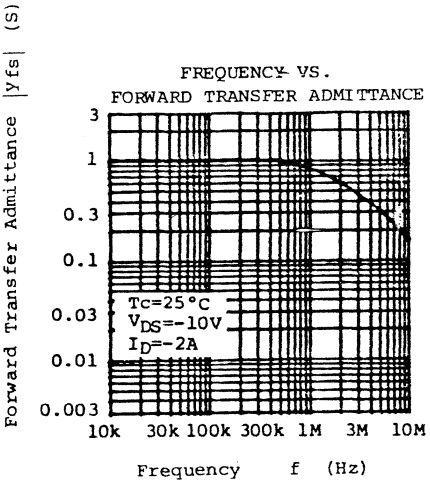
GATE TO SOURCE VOLTAGE VS.
DRAIN TO SOURCE VOLTAGE



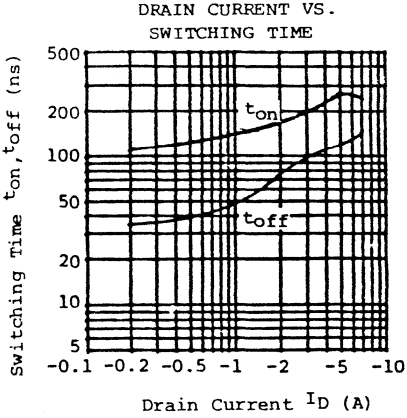
GATE TO SOURCE VOLTAGE VS.
INPUT CAPACITANCE



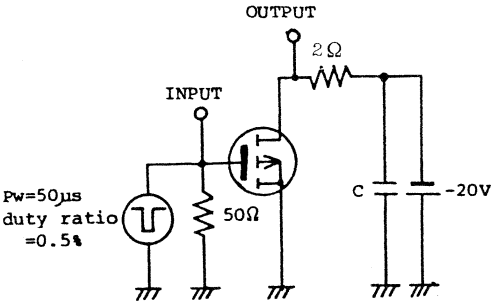
FREQUENCY VS.
FORWARD TRANSFER ADMITTANCE



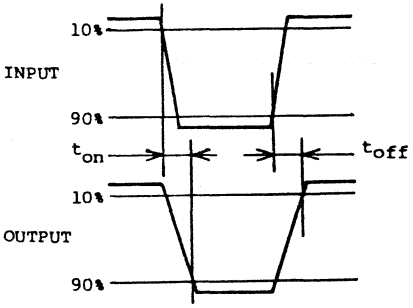
DRAIN CURRENT VS.
SWITCHING TIME



SWITCHING TIME TESTING CIRCUIT



RESPONSE WAVE FORM

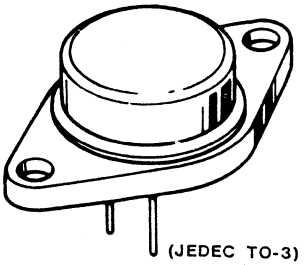


C: bypass capacitor

2SJ49H/50H

COMPLEMENT TO 2SK134H/135H)

SILICON P CHANNEL MOS FET
AUDIO POWER AMPLIFIER
CONVERTER


(JEDEC TO-3)

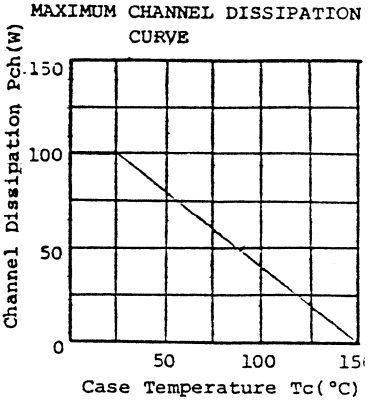
Features;

1. Superior High Frequency Characterictics.
2. High Speed Switching Characteristics.
3. Superior Durability.
4. Good Complementary Characteristics.
5. Enhancement-mode.

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating		Unit
		2SJ49 Ⓗ	2SJ50 Ⓗ	
Drain to Source Voltage	V_{DSX}	-140	-160	V
Gate to Source Voltage	V_{GSS}	±14	±14	V
Drain Current	I_D	-7	-7	A
Channel Dissipation	Pch*	100	100	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-65 ~+150	-65 ~+150	°C

* Value at Tc=25°C

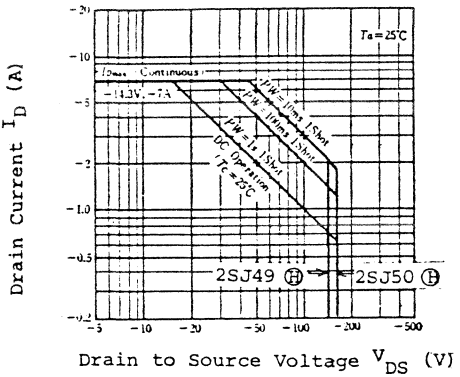


ELECTRICAL CHARACTERISTICS (Ta=25°C)

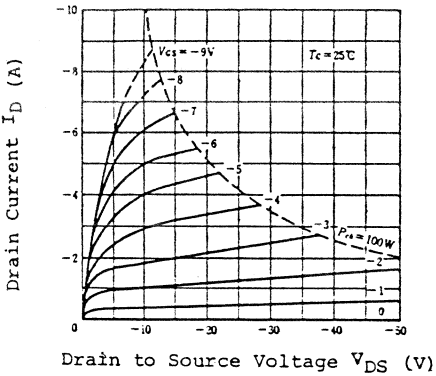
Item	Symbol	Test Condition	2SJ49 Ⓗ			2SJ50 Ⓗ			Uni
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	I_D=-10mA , V_{GS}=10V	-140	-	-	-160	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA , V_{DS}=0	±14	-	-	±14	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=-100mA , V_{DS}=-10V	-0.15	-	-1.45	-0.15	-	-1.45	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=-7A , V_{GD}=0	-	-	-12	-	-	-12	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-10V , I_D=-3A	0.7	1.0	1.4	0.7	1.0	1.4	S
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	900	-	-	900	-	PF
Output Capacitance	Coss		-	400	-	-	400	-	PF
Reverce Transfer Capacitance	Crss		-	40	-	-	40	-	PF
Turn on Time	t_{on}	V_{GS}=-10V, I_D=-2A, R_L=2Ω	-	150	-	-	150	-	ns
Turn-off Time	t_{off}		-	210	-	-	210	-	ns

* Pulse Test

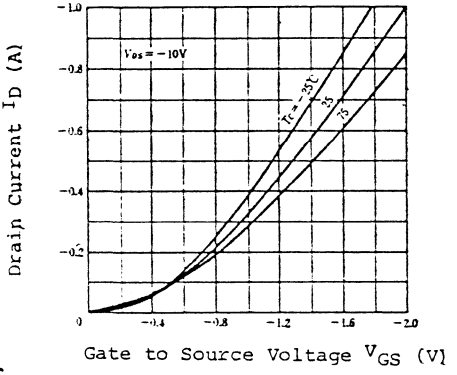
AREA OF SAFE OPERATION



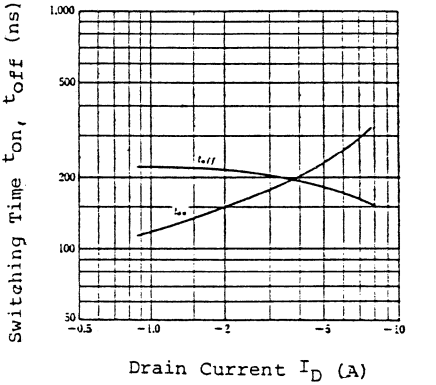
TYPICAL OUTPUT CHARACTERISTICS



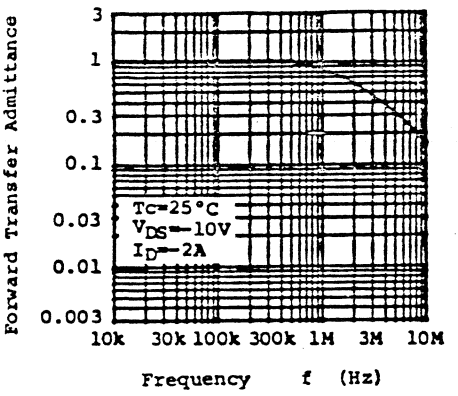
TYPICAL TRANSFER CHARACTERISTICS



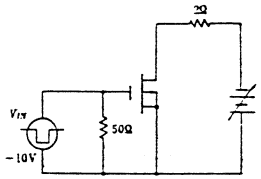
SWITCHING TIME VS. DRAIN CURRENT



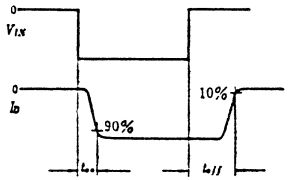
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



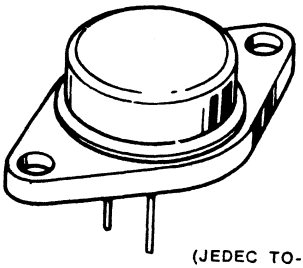
RESPONSE WAVE FORM



2SJ55/56
(COMPLEMENT TO 2SK175/176)

SILICON P-CHANNEL MOS FET

LOW FREQUENCY POWER AMPLIFIER



(JEDEC TO-3)

Features;

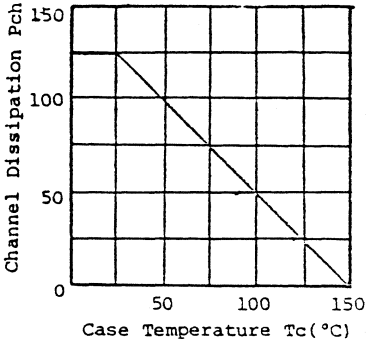
1. High Power Gain.
2. Excellent Frequency Response.
3. High Speed Switching.
4. Wide Area of Safe Operation.
5. Enhancement-mode.
6. Good Complementary Characteristics.
7. Equipped with Gate Protection Diodes.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating		Unit
		2SJ55	2SJ56	
Drain to Source Voltage	V_{DSX}	-180	-200	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	-8	-8	A
Channel Dissipation	Pch*	125	125	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-55～±150	-55～±150	°C

* Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE

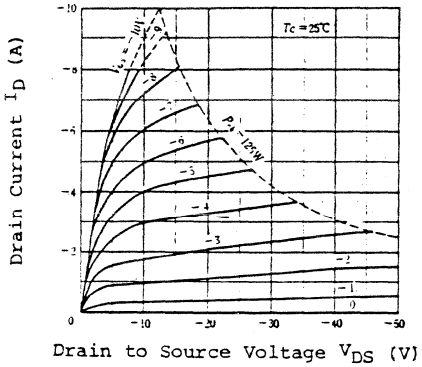


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

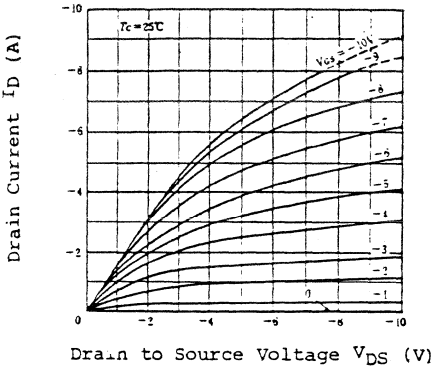
Item	Symbol	Test Condition	2SJ55			2SJ56			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	I_D=-10mA , V_{GS}=10V	-180	-	-	-200	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA , V_{DS}=0	±20	-	-	±20	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=-100mA , V_{DS}=-10V	-0.15	-	-1.45	-0.15	-	-1.45	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=-8A , V_{GD}=0	-	-	-12	-	-	-12	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-10V , I_D=-3A	0.7	1.0	1.4	0.7	1.0	1.4	S
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	1200	-	-	1200	-	PF
Output Capacitance	Coss		-	700	-	-	700	-	PF
Reverce Transfer Capacitance	Crss		-	60	-	-	60	-	PF
Turn on Time	t_{on}	V_{DD}=-30V , I_D=-4A	-	320	-	-	320	-	ns
Turn-off Time	t_{off}		-	120	-	-	120	-	ns

* Pulse Test

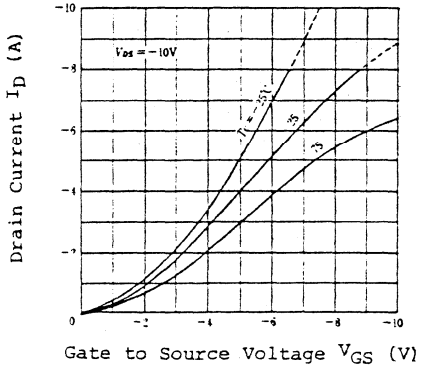
TYPICAL OUTPUT CHARACTERISTICS (1)



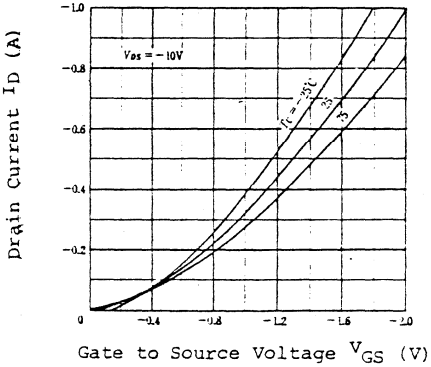
TYPICAL OUTPUT CHARACTERISTICS (2)



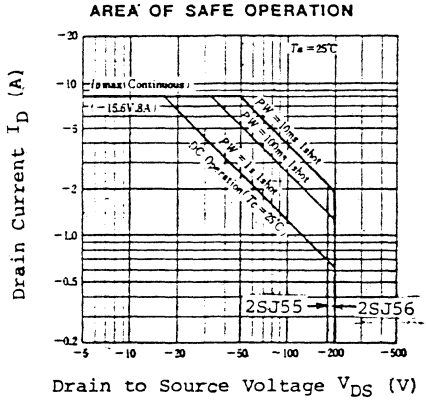
TYPICAL TRANSFER CHARACTERISTICS (1)



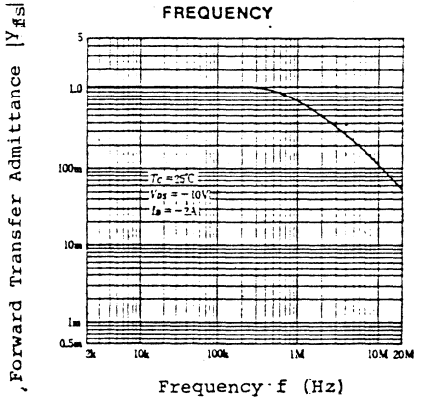
TYPICAL TRANSFER CHARACTERISTICS (2)



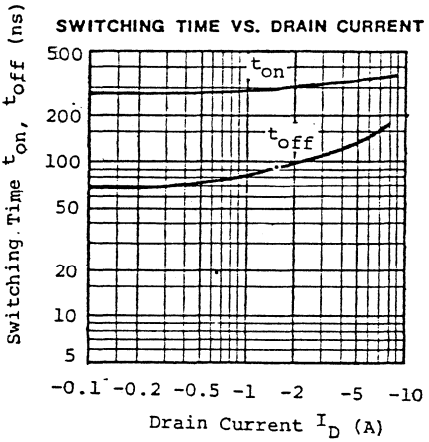
AREA OF SAFE OPERATION



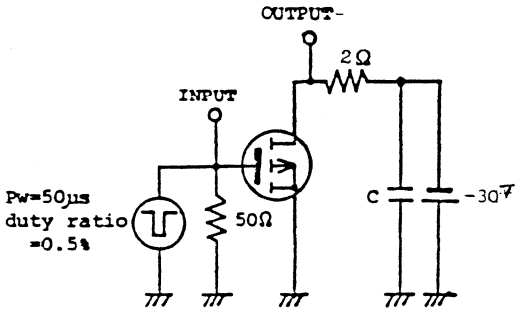
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME VS. DRAIN CURRENT

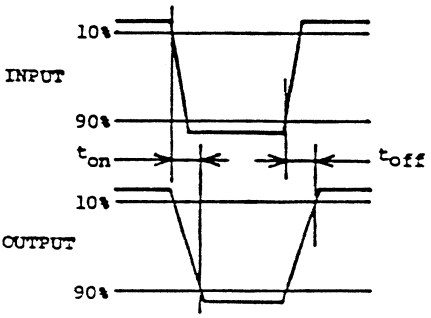


SWITCHING TIME TESTING CIRCUIT

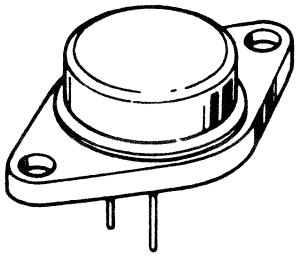


C: bypass capacitor,

RESPONSE WAVE FORM



SILICON P CHANNEL MOS FET
HIGH SPEED POWER SWITCHING
HIGH FREQUENCY POWER AMPLIFIER



(JEDEC TO-3)

Features;

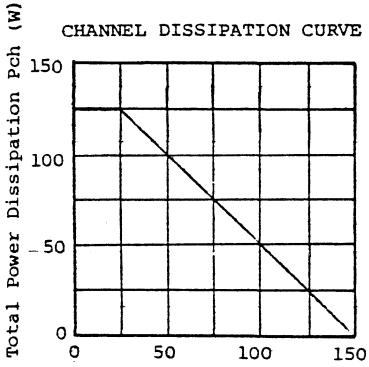
1. High Speed Switching
2. High Cutoff Frequency (f_C=1MHz)
3. Enhancement-Mode
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-200	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	-8	A
Channel Dissipation	Pch*	125	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-65～+150	°C

*Tc=25°C

CHANNEL DISSIPATION CURVE

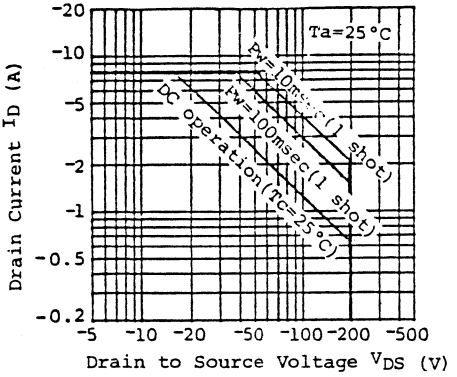


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

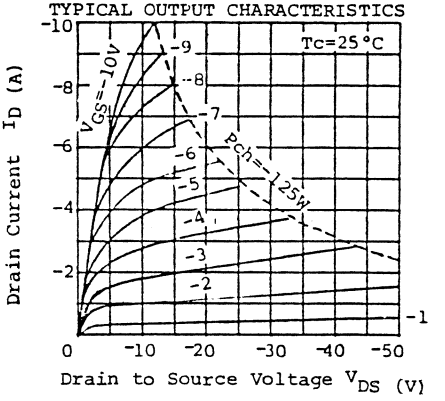
Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-10mA , V_{GS}=0	-200	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA , V_{DS}=0	±20	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=-100mA , V_{DS}=-10V	-0.55	-	-3.0	V
Drain Current	I_{DSS}	V_{DS}=-160V , V_{GS}=0	-	-	-3.0	mA
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=-4A , V_{GS}=-15V *	-	-	-6.0	V
Foward Transfer Admittance	$\|Y_{fs}\|$	V_{DS}=-10V , I_D=-3A *	0.7	1.0	1.4	S
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	1200	-	PF
Output Capacitance	Coss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	700	-	PF
Reverce Transfer Capacitance	Crss	V_{GD}=5V, f=1MHz	-	60	-	PF
Turn on Time	t_{on}	I_D=-2A, V_{GS}=-15V, R_L=15Ω	-	60	-	ns
Turn off Time	t_{off}		-	200	-	ns

* Pulse Test

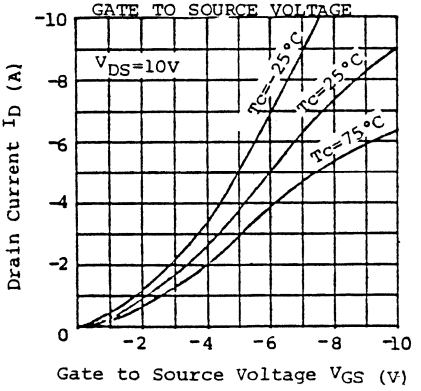
AREA OF SAFE OPERATION



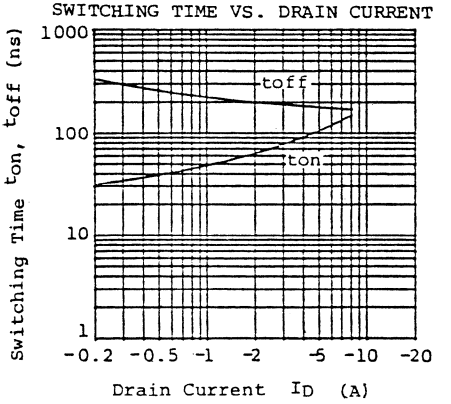
TYPICAL OUTPUT CHARACTERISTICS



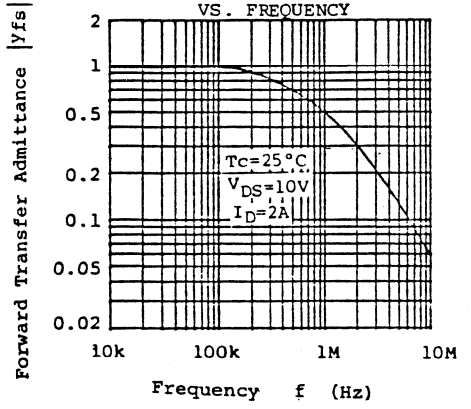
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



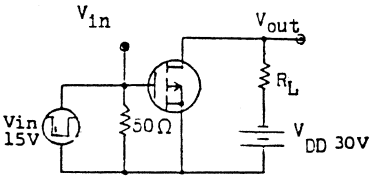
SWITCHING TIME VS. DRAIN CURRENT



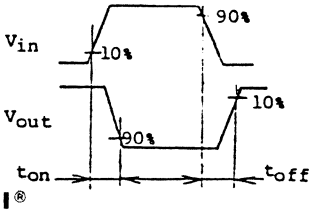
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



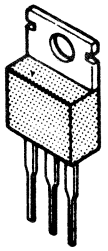
RESPONSE WAVE FORM



2SJ76/77/78/79
(COMPLEMENT TO 2SK213/214/215/216)

SILICON P-CHANNEL ENHANCEMENT MOS FET

LOW FREQUENCY AND HIGH FREQUENCY POWER AMPLIFIER, HIGH SPEED POWER SWITCHING



(JEDEC TO-220AB)

Features;

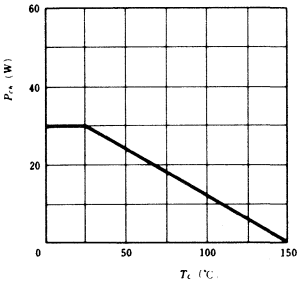
1. Suitable for direct mounting
2. High forward transfer addmittance
3. Excellent frequency response
4. Enhancement-mode

■ ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol		Unit
Drain to Source Voltage	V_{DSX}	−200 (2SJ79)	V
Gate to Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	−500	mA
Channel Dissipation	P_{ch}	1.75	W
	P_{ch}*	30	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−45 ~ +150	°C

* Value at $T_c = 25°C$

MAXIMUM CHANNEL DISSIPATION CURVE

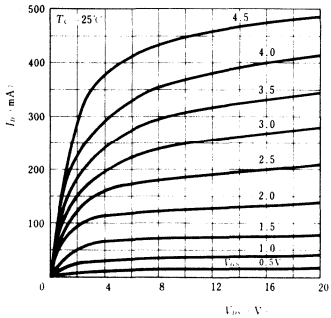


■ ELECTRICAL CHARACTERISTICS ($Ta = 25°C$)

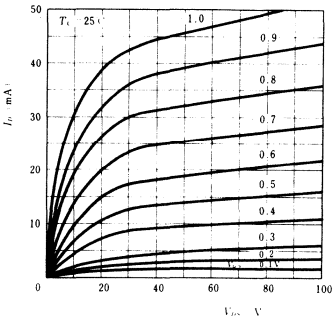
Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	$V_{GS} = 2V$, $I_D = -1mA$	—140 —160 —180 —200	–	–	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = \pm 10\mu A$, $V_{DS} = 0$	±15	–	–	V
Gate to Source Voltage	$V_{GS(off)}$	$V_{DS} = -10V$, $I_D = -10mA$ *	−0.2	–	−1.5	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	$I_D = -10mA$, $V_{GD} = 0$ *	–	–	−2	V
Forward Transfer Admittance	y_{fs}	$V_{DS} = -20V$, $I_D = -10mA$ *	–	35	–	mS
Input Capacitance	C_{iss}	$V_{DS} = -10V$, $I_D = -10mA$, $f = 1MHz$	–	120	–	pF
Feedback Capacitance	C_{rss}		–	4.8	–	pF

* Pulse Test

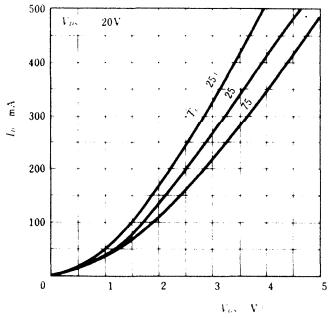
TYPICAL OUTPUT CHARACTERISTICS



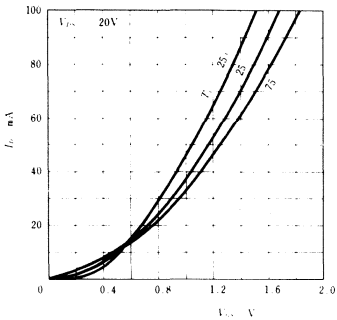
TYPICAL OUTPUT CHARACTERISTICS



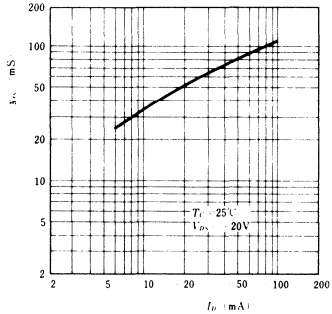
TYPICAL TRANSFER CHARACTERISTICS



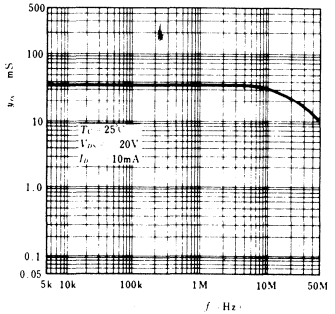
TYPICAL TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



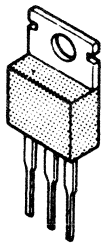
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



2SJ77K/79K

(COMPLEMENT TO 2SK214K/216K)

SILICON P CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER



(JEDEC TO-220AB)

Features;

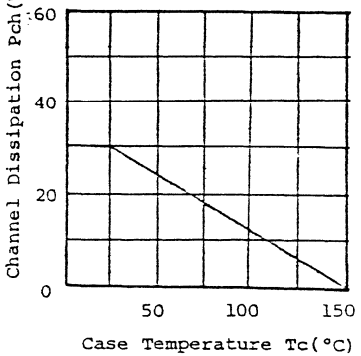
1. High Speed Switching
2. High Cutoff Frequency (f_c=30MHz)
3. High Breakdown Voltage
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating 2SJ77 Ⓚ	Rating 2SJ79 Ⓚ	Unit
Drain to Source Voltage	V_{DSX}	-160	-200	V
Gate to Source Voltage	V_{GSS}	±15	±15	V
Drain Current	I_D	-500	-500	A
Channel Dissipation	Pch	1.75	1.75	W
	Pch*	30	30	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-45~ +150	-45 ~ +150	°C

* Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE

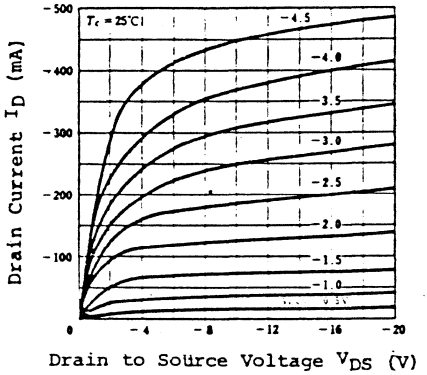


■ ELECTRICAL CHARACTERISTICS (Tc=25°C)

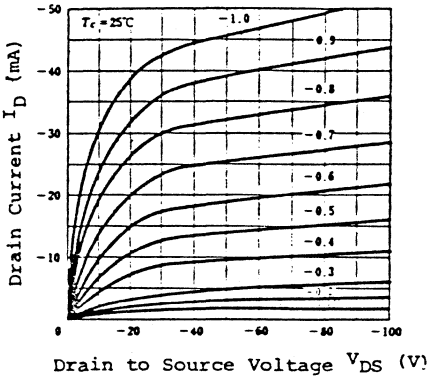
Item	Symbol	Test Condition	2SJ77 Ⓚ min	2SJ77 Ⓚ typ	2SJ77 Ⓚ max	2SJ79 Ⓚ min	2SJ79 Ⓚ typ	2SJ79 Ⓚ max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	V_{GS}=2V, I_D=-1mA	-160	—	—	-200	—	—	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_{GS}=±10uA, V_{DS}=0	±15	—	—	±15	—	—	V
Gate to Source Voltage	$V_{GS(on)}$	V_{DS}=-10V, I_D=-10mA *	-0.2	—	-1.5	-0.2	—	-1.5	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=-10mA, V_{GD}=0 *	—	—	-2.0	—	—	-2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-20V, I_D=-10mA *	—	35	—	—	35	—	S
Input Capacitance	Ciss	V_{DS}=-10V, I_D=-10mA' f=1MHz	—	120	—	—	120	—	PF
Output Capacitance	Crss		—	4.8	—	—	4.8	—	PF

* Pulse Test

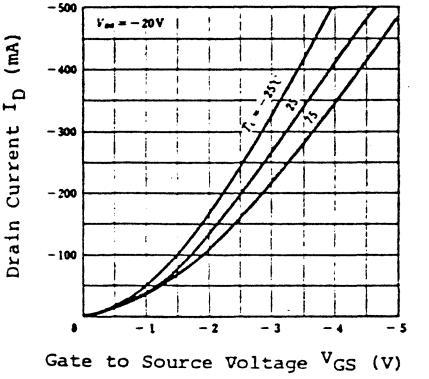
TYPICAL OUTPUT CHARACTERISTICS (1)



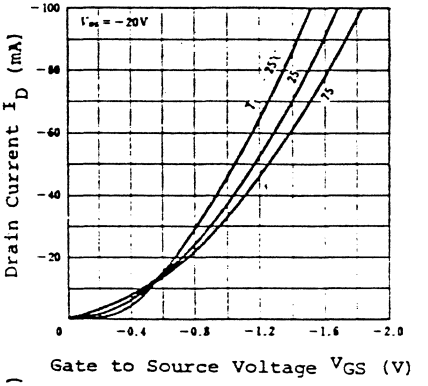
TYPICAL OUTPUT CHARACTERISTICS (2)



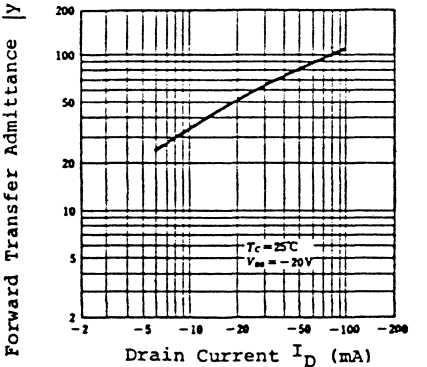
TYPICAL TRANSFER CHARACTERISTICS (1)



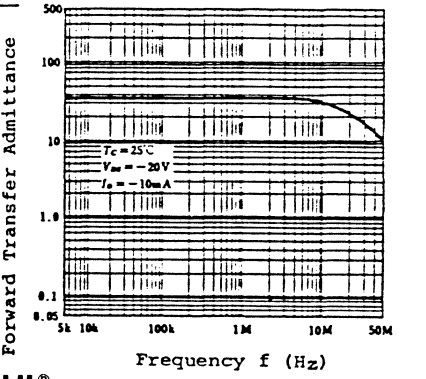
TYPICAL TRANSFER CHARACTERISTICS (2)



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



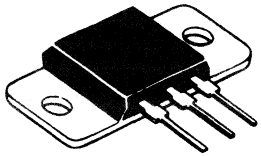
2SJ81

(COMPLEMENT TO 2SK225)

SILICON P CHANNEL MOS FET
LOW FREQUENCY POWER AMPLIFIER

Features;

1. High Power Gain
2. Excellent Frequency Response
3. High Speed Switching
4. Thermal Stability and no secondary Breakdown

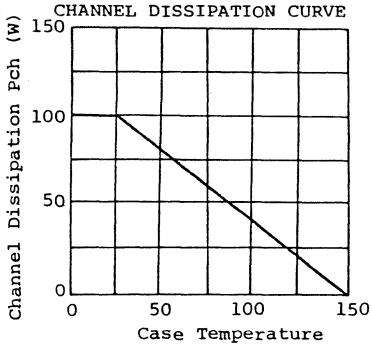


(HPAK)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSX}	-120	V
Gate to Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	-7	A
Channel Dissipation	Pch*	100	W
Storage Temperature	T_{stg}	-45~+150	°C

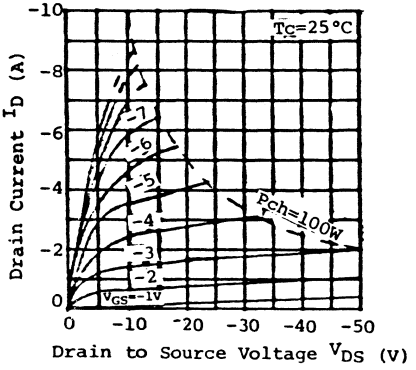
*Tc=25°C



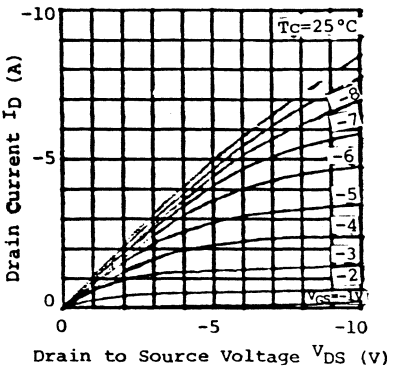
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	I_D=-1mA, V_{GS}=10V	-120	-	-	V
Gate to Source Cutoff Curernt	I_{GSS1}	V_{GS}=20V, V_{DS}=0	-	-	1	μA
Gate to Source Cutoff Current	I_{GSS2}	V_{GS}=-20V, V_{DS}=0	-	-	-1	μA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=-100mA, V_{DS}=0	-0.15	-	-1.45	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=-7A, V_{GD}=0	-	-	-12	V
Foward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-10V, I_D=-3A	0.7	1.0	1.4	S
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	780	-	pF
Turn on Time	t_{on}	V_{DD}=-20V, I_D=-4A	-	400	-	ns
Turn off Time	t_{off}		-	170	-	ns

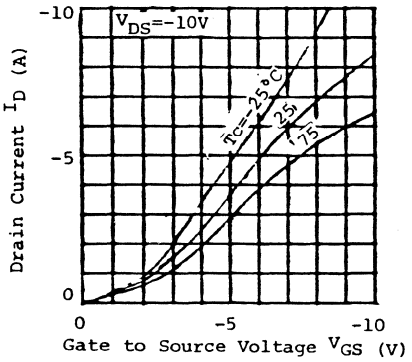
TYPICAL OUTPUT CHARACTERISTICS (1)



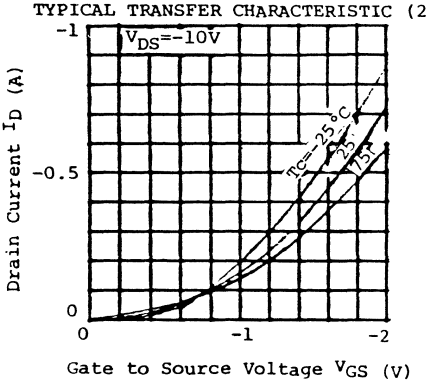
TYPICAL OUTPUT CHARACTERISTICS (2)



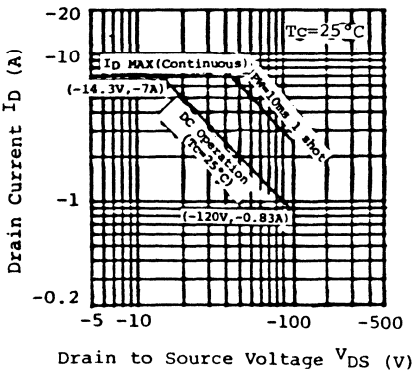
TYPICAL TRANSFER CHARACTERISTIC (1)



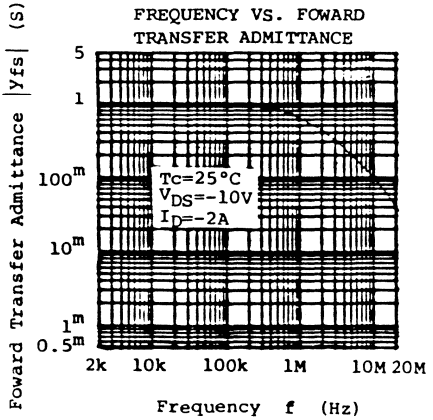
TYPICAL TRANSFER CHARACTERISTIC (2)



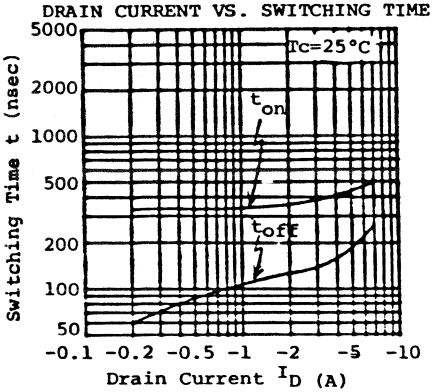
AREA OF SAFE OPERATION



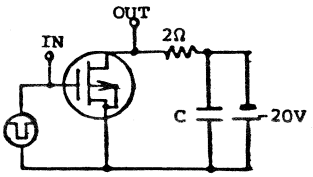
FREQUENCY VS. FOWARD TRANSFER ADMITTANCE



DRAIN CURRENT VS. SWITCHING TIME



SWITCHING TIME TEST CIRCUIT

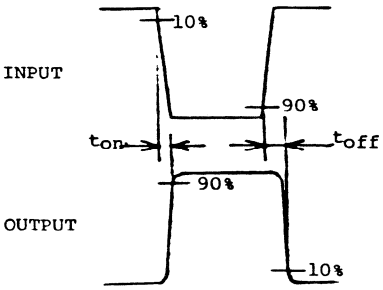


C : Bypass Capacitor

PW=50μs

duty ratio=0.5%

RESPONSE WAVE FORM

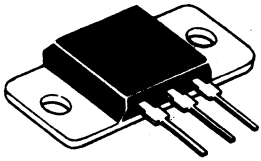


2SJ82/83

(COMPLEMENT TO 2SK226/227)

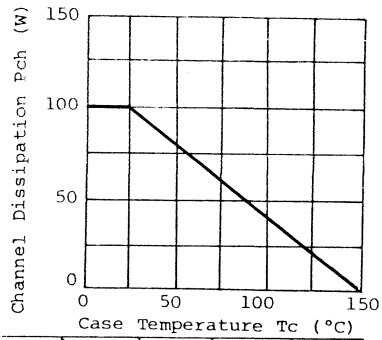
SILICON P-CHANNEL MOS FET
LOW FREQUENCY POWER AMPLIFIER
Features;

1. High Power Gain.
2. Excellent Frequency Response.
3. High Speed Switching.
4. Wide Area of Safe Operation.
5. Enhancement-mode.
6. Good Complementary Characteristics.
7. Equipped with Gate Protection Diodes.



(HPAK)

MAXIMUM CHANNEL DISSIPATION CURVE



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSX}	-160	V
Gate to Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	-7	A
Channel Dissipation	Pch*	100	W
Storage Temperature	T_{stg}	-45~+150	°C

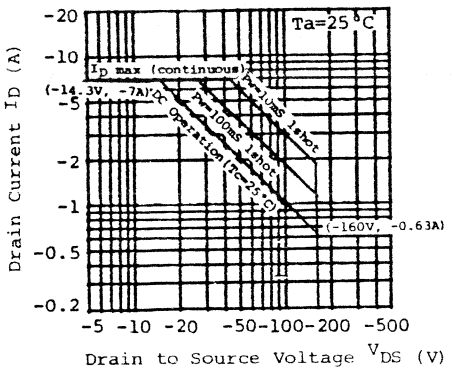
*Tc=25°C

■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

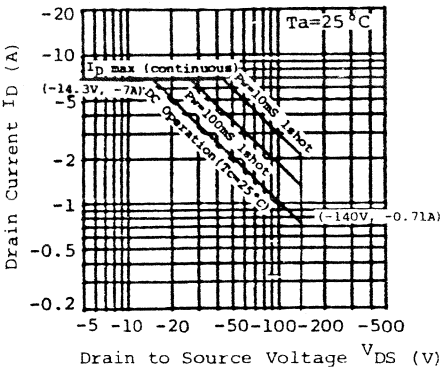
Item		Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	2SJ82	$V_{(BR)DSX}$	I_D=-10mA, V_{GS}=10V	-140	-	-	V
	2SJ83			-160	-	-	V
Gate to Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	-	-	V
Gate to Source Cutoff Voltage		$V_{GS(off)}$	I_D=-100mA, V_{DS}=-10V	-0.15	-	-1.45	V
Drain to Source Saturation Voltage		$V_{DS(sat)}$	I_D=-7A, V_{GD}=0 *	-	-	-12	V
Forward Transfer Admittance		$\|Yfs\|$	V_{DS}=-10V, I_D=-3A *	0.7	1.0	1.4	S
Input Capacitance		Ciss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	900	-	pF
Output Capacitance		Coss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	400	-	pF
Reverse Transfer Capacitance		Crss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	40	-	pF
Turn on Time		t_{on}	V_{DD}=-20V, I_D=4A	-	230	-	ns
Turn off Time		t_{off}		-	110	-	ns

*Pulse Test

A.S.O. CHARACTERISTICS — 2SJ83

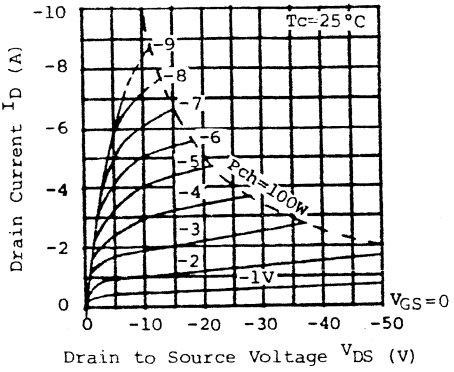


A.S.O. CHARACTERISTICS — 2SJ82

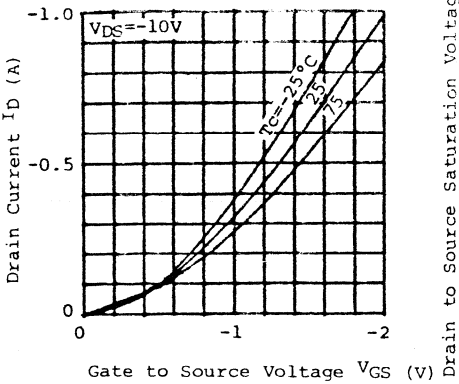


GENERAL CHARACTERISTICS —2SJ82/83

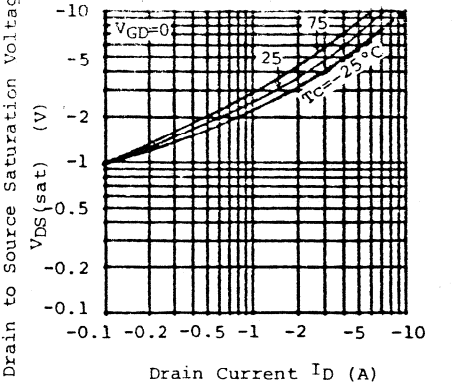
TYPICAL OUTPUT CHARACTERISTICS



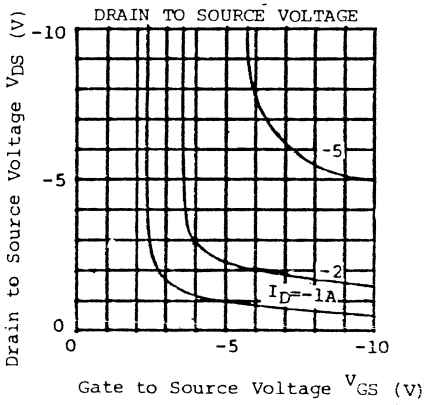
TYPICAL TRANSFER CHARACTERISTICS



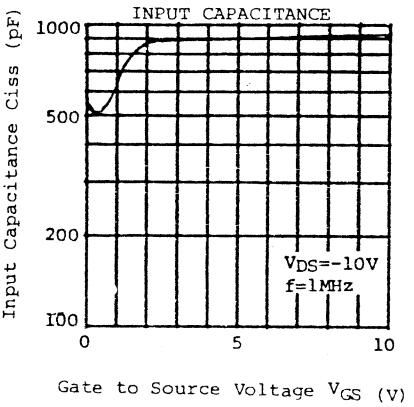
DRAIN CURRENT VS. DRAIN TO SOURCE SATURATION VOLTAGE



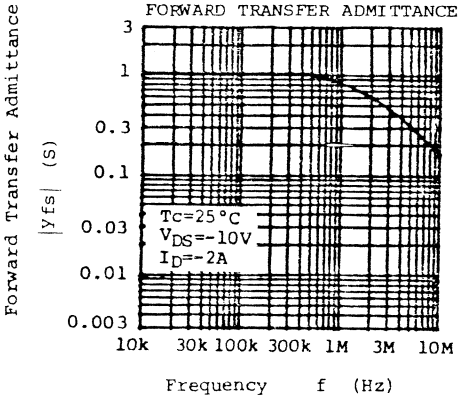
GATE TO SOURCE VOLTAGE VS
DRAIN TO SOURCE VOLTAGE



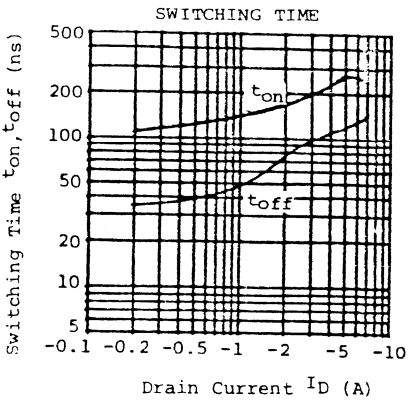
GATE TO SOURCE VOLTAGE VS.
INPUT CAPACITANCE



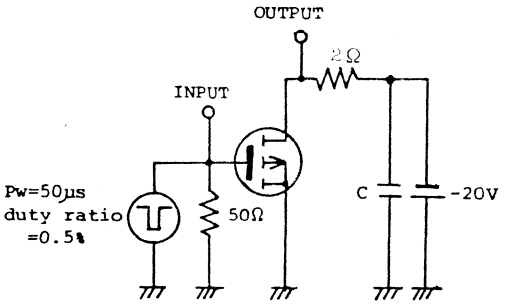
FREQUENCY VS.
FORWARD TRANSFER ADMITTANCE



DRAIN CURRENT VS.
SWITCHING TIME

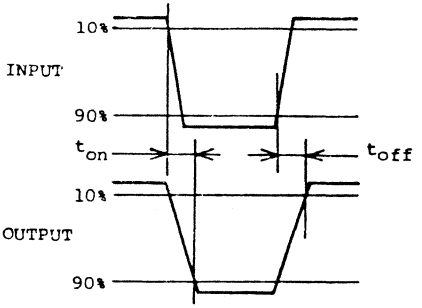


SWITCHING TIME TESTING CIRCUIT



C: bypass capacitor

RESPONSE WAVE FORM

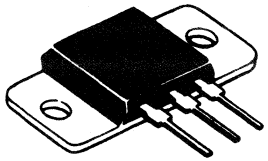


2SJ96
(COMPLEMENT TO 2SK286)

SILICON P-CHANNEL ENHANCEMENT-MODE MOS FET
LOW FREQUENCY·HIGH FREQUENCY POWER AMPLIFIER,
HIGH SPEED POWER SWITCHING

Features;

1. Low Saturation Voltage.(0.5Ω typ R_{ch})
2. Excellent Frequency Response.
3. High Speed Switching.
4. High Mutual Condactance.
5. Excellent Complementary Characteristics.

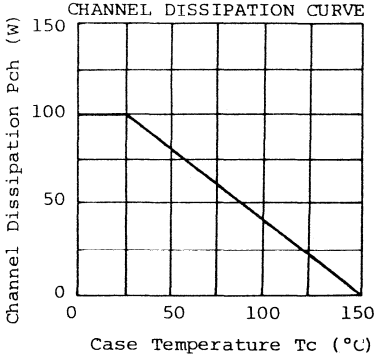


(HPAK)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSX}	-60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	-8	A
Channel Dissipation	Pch*	100	W
Channel Temperature	Tch	150	°C
Storage Temprature	Tstg	-45～+150	°C

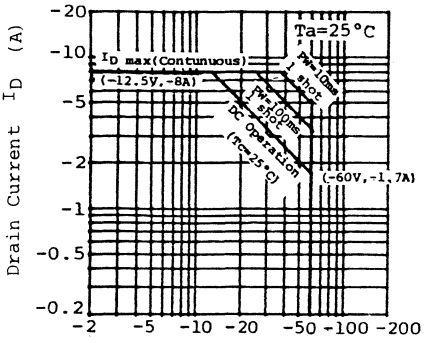
*Tc=25°C



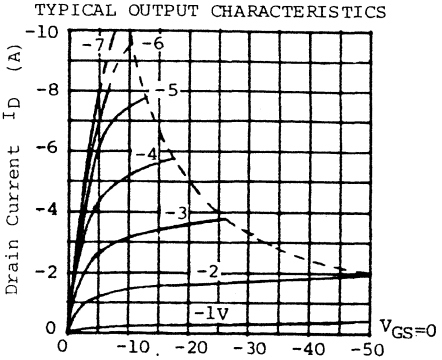
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Cutoff Current	I_{DSX}	V_{DS}=-60V, V_{GS}=10V	-	-	-1	mA
Gate to Source Cutoff Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	±1	μA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS}=-10V, I_D=-10mA	-0.2	-	-1.5	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	V_{GS}=-15V, I_D=-5A	-	-2.5	-4.0	V
Foward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-10V, I_D=-3A	1.0	1.6	2.5	S
Turn on Time	t_{on}	V_{GS}=-10V, I_D=4A	-	100	-	ns
Turn off Time	t_{off}	V_{GS}=-10V, I_D=-4A	-	250	-	ns
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=-10V, f=1MHz	-	850	-	pF

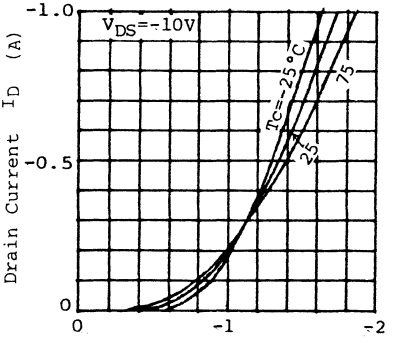
AREA OF SAFE OPERATION



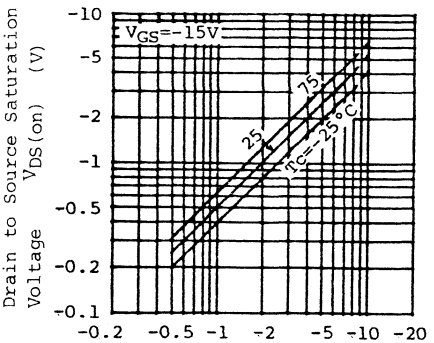
TYPICAL OUTPUT CHARACTERISTICS



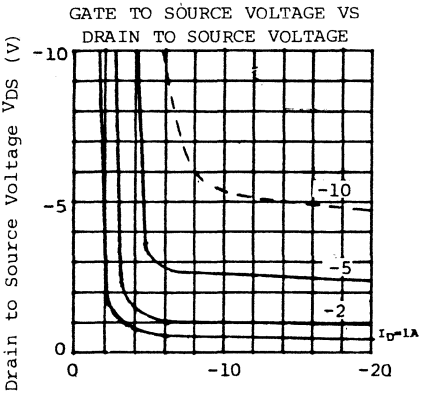
TYPICAL TRANSFER CHARACTERISTICS



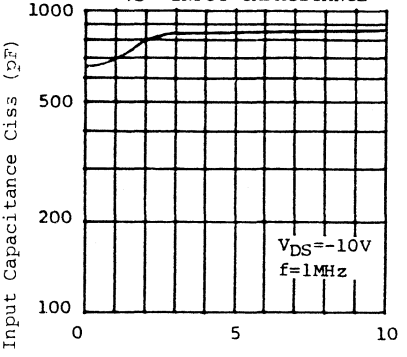
DRAIN CURRENT VS. DRAIN TO SOURCE SATURATION VOLTAGE



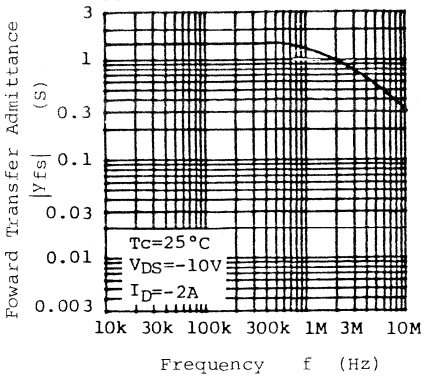
GATE TO SOURCE VOLTAGE VS DRAIN TO SOURCE VOLTAGE



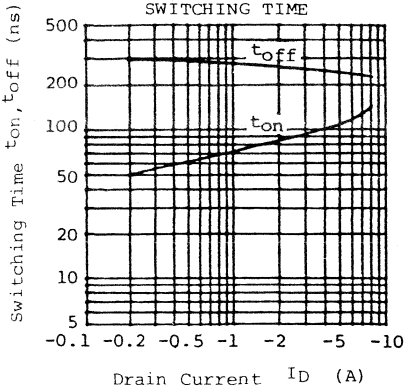
GATE TO SOURCE VOLTAGE VS INPUT CAPACITANCE



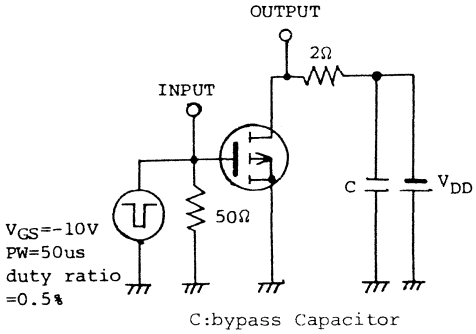
FREQUENCY VS.
FOWARD TRANSFER ADMITTANCE



DRAIN CURRENT VS.
SWITCHING TIME

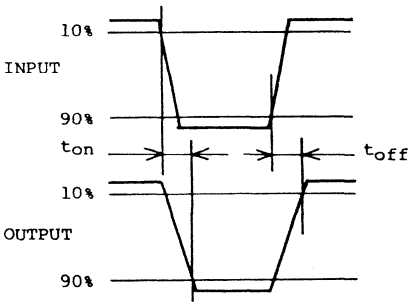


SWITCHING TIME TESTING CIRCUIT



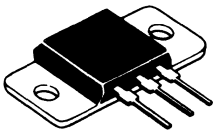
C:bypass Capacitor

RESPONSE WAVE FORM



2JS99/100

SILICON P-CHANNEL ENHANCEMENT MOS FET
LOW FREQUENCY POWER AMPLIFIER,
HIGH SPEED AND POWER SWITCHING
Complementary pair with 2SK343,2SK344



(HPAK)

Features;

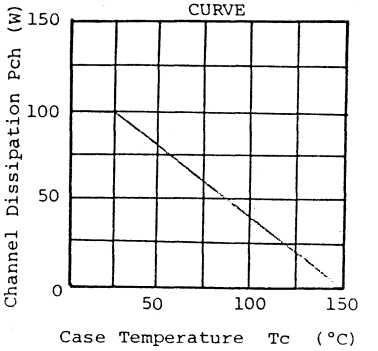
1. Low On-Resistance.
2. High Speed Switching.
3. No Secondary Breakdown.
4. Good Complementary Characteristics.

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating		Unit
		2SJ99	2SJ100	
Drain to Source Voltage	V_{DSS}	-140	-160	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	-8	-8	A
Drain Peak Current	$I_{D(peak)}$	-12	-12	A
Channel Dissipation	Pch*	100	100	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	T_{stg}	-45~+150	-45~+150	°C

*Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE



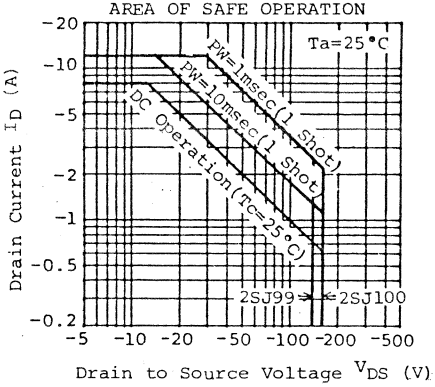
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	2SJ99			2SJ100			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-10mA, V_{GS}=0	-140	-	-	-160	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	-1	-	-	-1	μA
Drain Current	I_{DSS}	J99 V_{DS}=-120V, V_{GS}=0	-	-	-1	-	-	-	mA
		J100 V_{DS}=-140V, V_{GS}=0	-	-	-	-	-	-1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS}=-10V, I_D=-1mA	-2.0	-	-5.0	-2.0	-	-5.0	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	V_{GS}=-15V, I_D=-4A*	-	-1.6	-2.0	-	-0.6	-2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-10V, I_D=-4A*	1.0	1.8	-	1.0	1.8	-	S
Input Capacitance	Ciss	V_{DS}=-10V, V_{GS}=0, f=1MHz	-	1050	-	-	1050	-	pF
Output Capacitance	Coss		-	450	-	-	450	-	pF
Reverce Transfer Capacitance	Crss		-	80	-	-	80	-	pF
Turn on Time	ton	V_{GS}=-15V, I_D=-2A	-	120	-	-	120	-	ns
Turn off Time	toff		-	120	-	-	120	-	ns

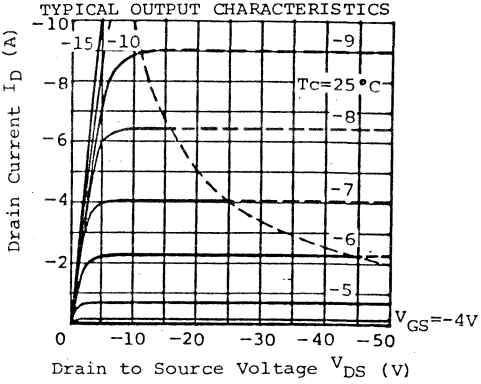
*Pulse Test

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

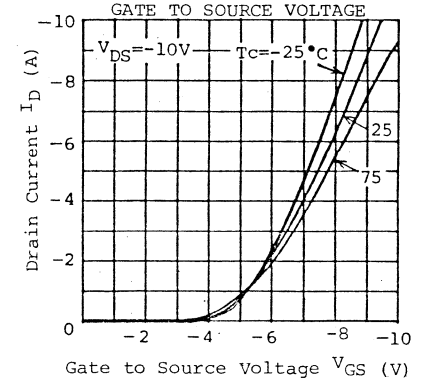
AREA OF SAFE OPERATION



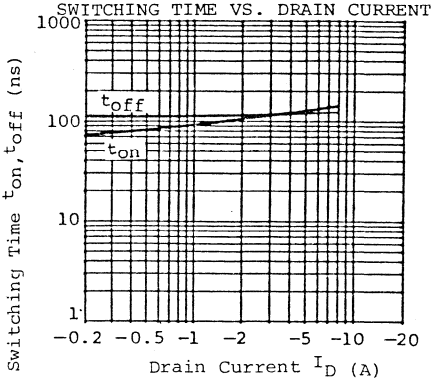
TYPICAL OUTPUT CHARACTERISTICS



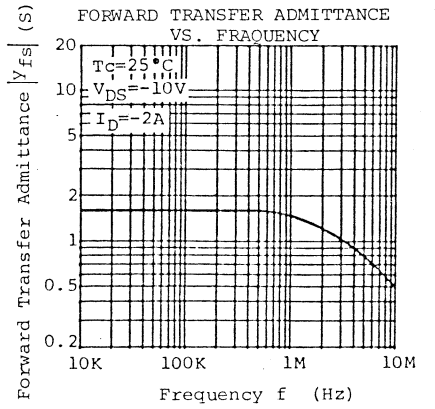
DRAIN CURRENT VS.
GATE TO SOURCE VOLTAGE



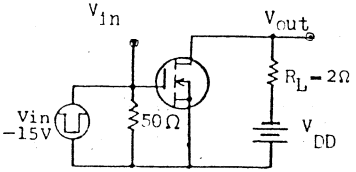
SWITCHING TIME VS. DRAIN CURRENT



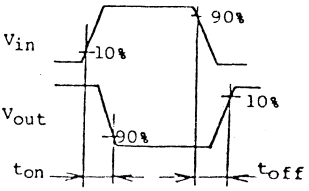
FORWARD TRANSFER ADMITTANCE
VS. FRAQUENCY



SWITCHING TIME TEST CIRCUIT

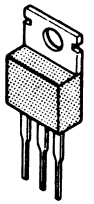


RESPONSE WAVE FORM



2SJ101/102

SILICON P CHANNEL MOS FET
LOW FREQUENCY POWER AMPLIFIER
HIGH SPEED POWER SWITCHING
Complementary pair with 2SK345,SK346.



(JEDEC TO-220AB)

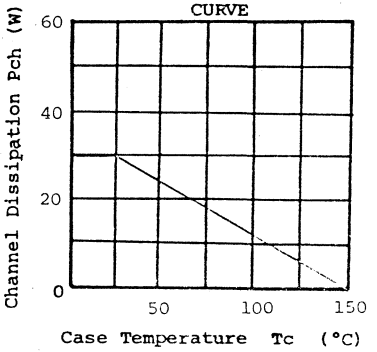
Features;
1. Low On-Resistance.
2. High Speed Switching.
3. No Secondary Breakdown.
4. Good Complementary Characteristics.

ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating		Unit
		2SJ101	2SJ102	
Drain to Source Voltage	V_{DSS}	-40	-60	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	-5	-5	A
Drain Peak Current	$I_{D(peak)}$	-10	-10	A
Channel Dissipation	Pch*	30	30	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-45 ~ +150	-45 ~ +150	°C

*Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE



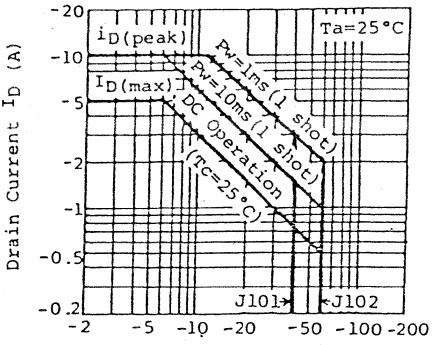
ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	2SJ101			2SJ102			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	-40	-	-	-60	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0	-	-	-1	-	-	-1	μA
Drain Current	I_{DSS} J101	V_{DS}=-30V, V_{GS}=0	-	-	-1	-	-	-	mA
	I_{DSS} J102	V_{DS}=-50V, V_{GS}=0	-	-	-	-	-	-1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V , I_D=-1mA	-2.0	-	-5.0	-2.0	-	-5.0	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	V_{GS}=-15V , I_D=-3A	-	-0.9	-1.2	-	-0.9	-1.2	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=-10V , I_D=-3A	0.5	1.0	-	0.5	1.0	-	S
Input Capacitance	Ciss	V_{DS}=-10V, V_{GS}=0, f=1MHz	-	700	-	-	700	-	pF
Output Capacitance	Coss		-	300	-	-	300	-	pF
Reverce Transfer Capacitance	Crss		-	60	-	-	60	-	pF
Turn on Time	ton	V_{GS}=-15V , I_D=-2A	-	60	-	-	60	-	ns
Turn off Time	toff		-	80	-	-	80	-	ns

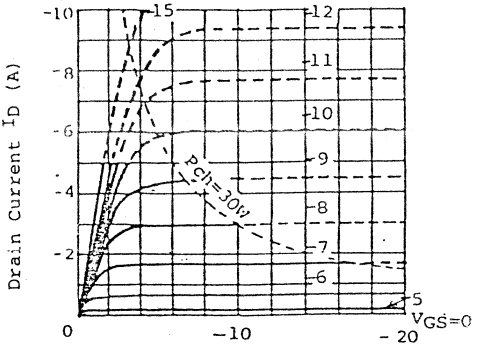
*Pulse Test

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

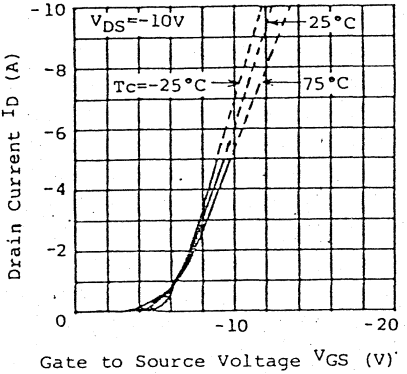
AREA OF SAFE OPERATION



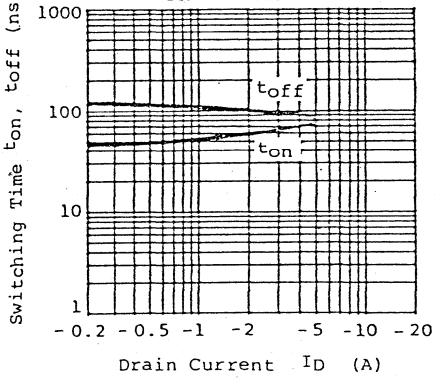
TYPICAL OUTPUT CHARACTERISTICS



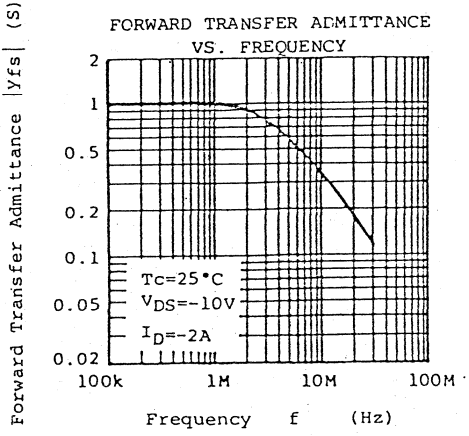
TYPICAL TRANSFER CHARACTERISTICS



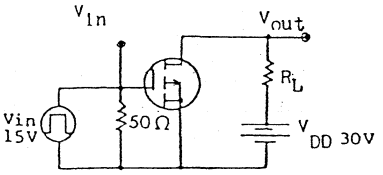
SWITCHING TIME VS. DRAIN CURRENT



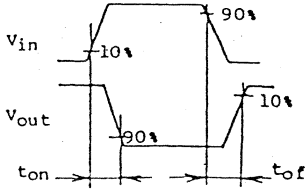
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



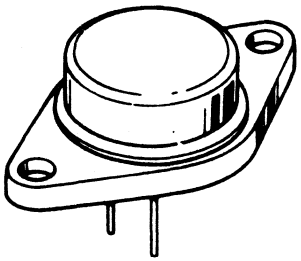
SWITCHING TIME TESTING CIRCUIT



RESPONSE WAVE FORM



2SK133/134/135
(COMPLEMENT TO 2SJ48/49/50)



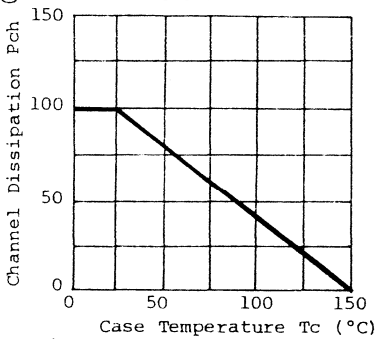
(JEDEC TO-3)

SILICON N-CHANNEL MOS FET
LOW FREQUENCY POWER AMPLIFIER

Features;

1. High Power Gain.
2. Excellent Frequency Response.
3. High Speed Switching.
4. Wide Area of Safe Operation.
5. Enhancement-mode.
6. Good Complementary Characteristics.
7. Equipped with Gate Protection Diodes.

MAXIMUM CHANNEL DISSIPATION CURVE



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage (2SK135)	V_{DSX}	160	V
Gate to Source Voltage	V_{GSS}	±14	V
Drain Current	I_D	7	A
Channel Dissipation	Pch*	100	W
Storage Temperature	T_{stg}	-55~+150	°C

*Tc=25°C

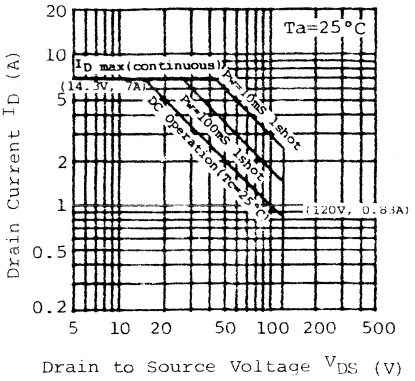
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	2SK133	$V_{(BR)DSX}$	I_D=10mA, V_{GS}=-10V	120	-	-	V
	2SK134			140			
	2SK135			160			
Gate to Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±14	-	-	V
Gate to Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.15	-	1.45	V
Drain to Source Saturation Voltage		$V_{DS(sat)}$	I_D=7A, V_{GD}=0 *	-	-	12	V
Forward Transfer Admittance		$\|y_{fs}\|$	V_{DS}=10V, I_D=3A *	0.7	1.0	1.4	S
Input Capacitance		Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	600	-	pF
Output Capacitance		Coss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	350	-	pF
Reverse Transfer Capacitance		Crss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	10	-	pF
Turn on Time		ton	V_{DD}=20V, I_D=4A	-	180	-	ns
Turn off Time		toff		-	60	-	ns

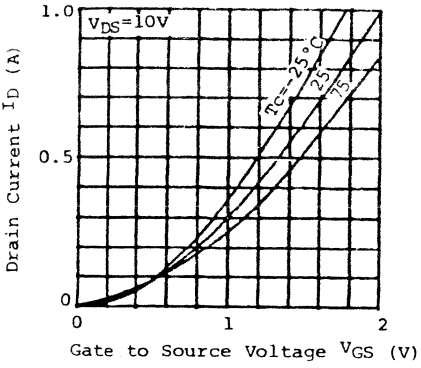
*Pulse Test

2SK133

AREA OF SAFE OPERATION

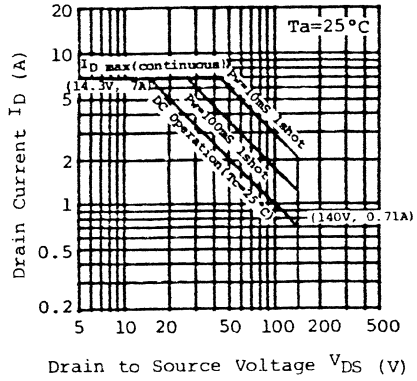


TYPICAL TRANSFER CHARACTERISTICS

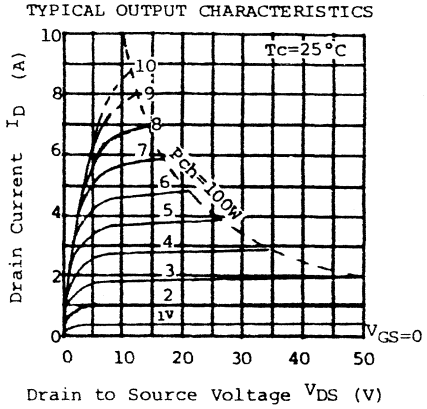


2SK134

AREA OF SAFE OPERATION

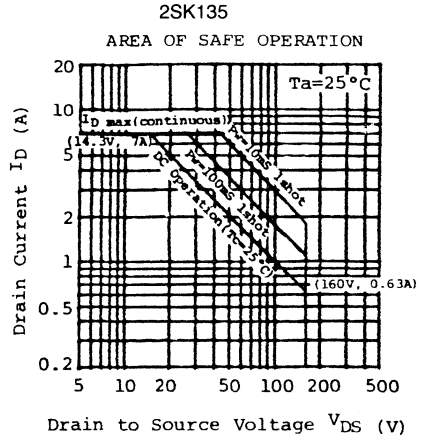


TYPICAL OUTPUT CHARACTERISTICS

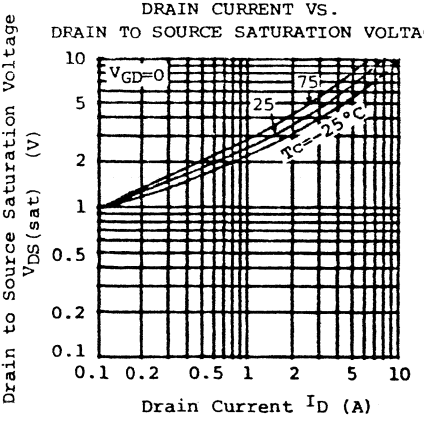


2SK135

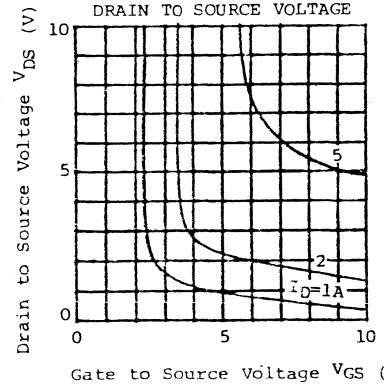
AREA OF SAFE OPERATION



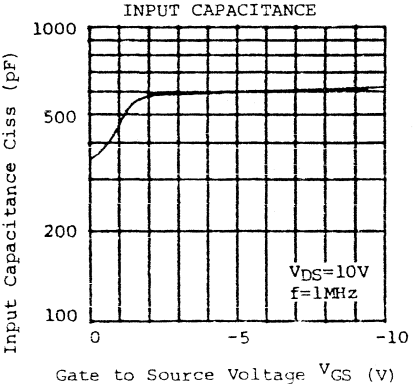
DRAIN CURRENT VS.
DRAIN TO SOURCE SATURATION VOLTAGE



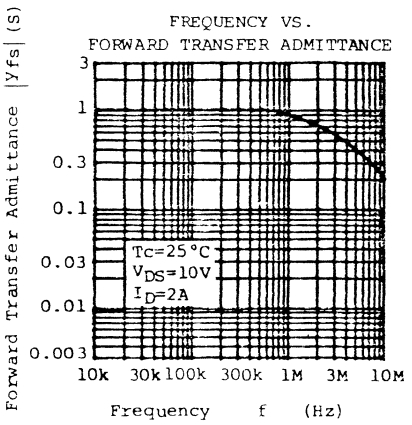
GATE TO SOURCE VOLTAGE VS.
DRAIN TO SOURCE VOLTAGE



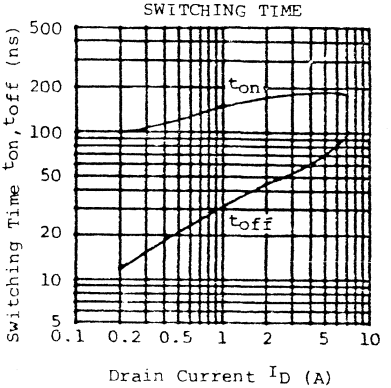
GATE TO SOURCE VOLTAGE VS.
INPUT CAPACITANCE



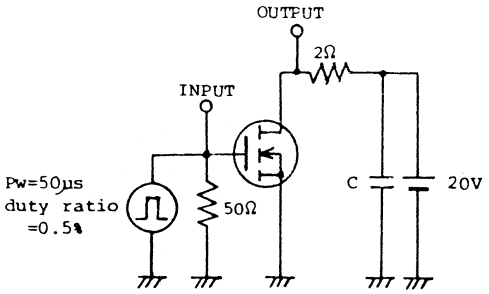
FREQUENCY VS.
FORWARD TRANSFER ADMITTANCE



DRAIN CURRENT VS.
SWITCHING TIME

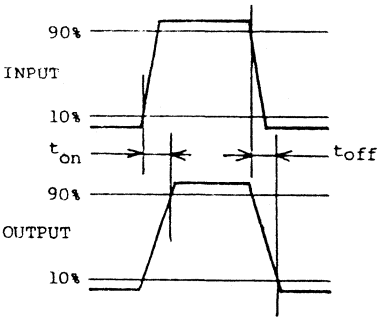


SWITCHING TIME TESTING CIRCUIT



C:bypass capacitor

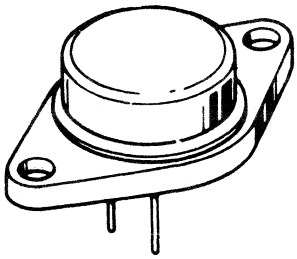
RESPONSE WAVE FORM



2SK134H/135H

(COMPLEMENT TO 2SJ49H/50H)

SILICON N CHANNEL MOS FET
AUDIO POWER AMPLIFIER
CONVERTER



(JEDEC TO-3)

Features;

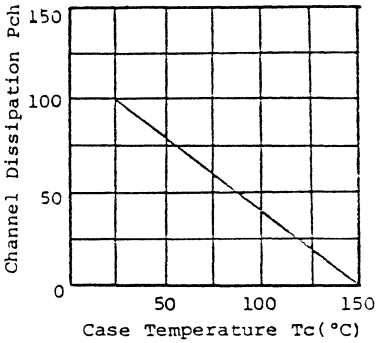
1. Superior High Frequency Characteristics.
2. High Speed Switching Characteristics.
3. Superior Durability.
4. Good Complementary Characteristics.
5. Enhancement-mode.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating		Unit
		2SK134 Ⓗ	2SK135 Ⓗ	
Drain to Source Voltage	V_{DSX}	140	160	V
Gate to Source Voltage	V_{GSS}	±14	±14	V
Drain Current	I_D	7	7	A
Channel Dissipation	Pch*	100	100	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-65～+150	-65～+150	°C

* Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE

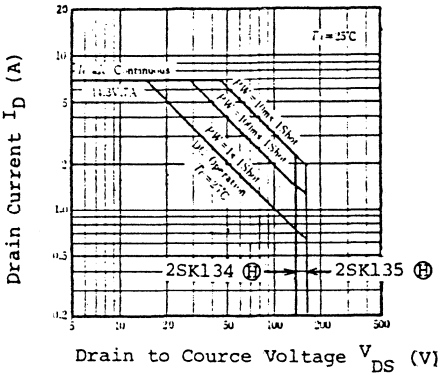


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

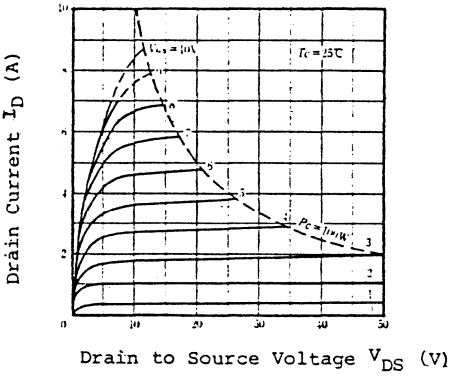
Item	Symbol	Test Condition	2SK134 Ⓗ			2SK135 Ⓗ			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	I_D=10mA , V_{GS}=-10V	140	-	-	160	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA , V_{DS}=0	±14	-	-	±14	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=100mA , V_{DS}=10V	0.15	-	1.45	0.15	-	1.45	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=7A , V_{GD}=0	-	-	12	-	-	12	V
Forward Transfer Admittance	$\|Y_{fs}\|$	V_{DS}=10V , I_D=3A	0.7	1.0	1.4	0.7	1.0	1.4	S
Input Capacitance	Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	600	-	-	600	-	PF
Output Capacitance	Coss		-	350	-	-	350	-	PF
Reverce Transfer Capacitance	Crss		-	10	-	-	10	-	PF
Turn on Time	t_{on}	V_{GS}=10V , I_D=2A , R_L=2Ω	-	90	-	-	90	-	ns
Turn-off-Time	t_{off}		-	110	÷	-	110	-	ns

* Pulse Test

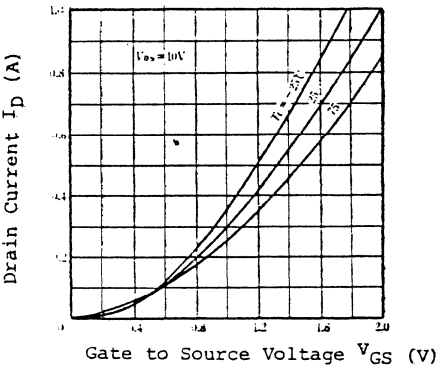
AREA OF SAFE OPERATION



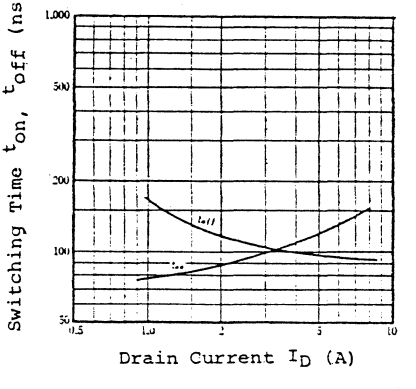
TYPICAL OUTPUT CHARACTERISTICS



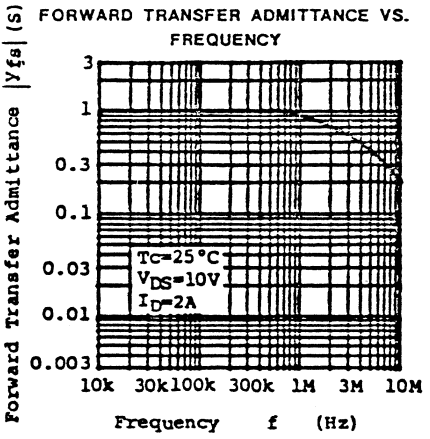
TYPICAL TRANSFER CHARACTERISTICS



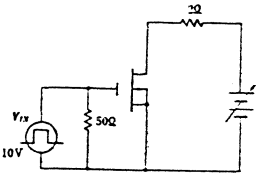
SWITCHING TIME VS. DRAIN CURRENT



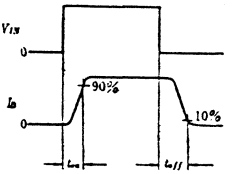
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM



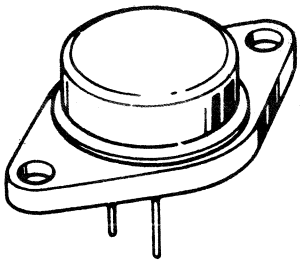
2SK175/176

(COMPLEMENT TO 2SJ55/56)

SILICON N-CHANNEL MOS FET
LOW FREQUENCY POWER AMPLIFIER

Features;

1. High Power Gain.
2. Excellent Frequency Response.
3. High Speed Switching.
4. Wide Area of Safe Operation.
5. Enhancement-mode.
6. Good Complementary Characteristics.
7. Equipped with Gate Protection Diodes.



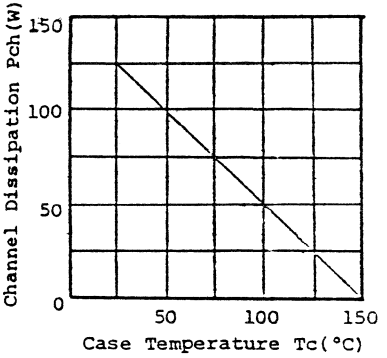
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating		Unit
		2SK175	2SK176	
Drain to Source Voltage	V_{DSX}	180	200	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	8	8	A
Channel Dissipation	Pch*	125	125	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-55～+150	-55～+150	°C

* Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE

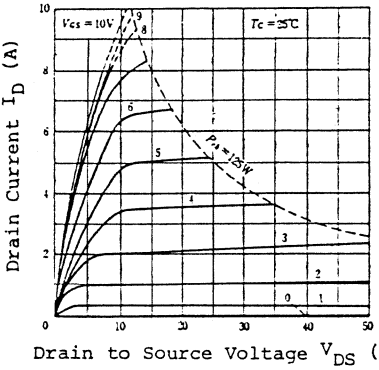


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

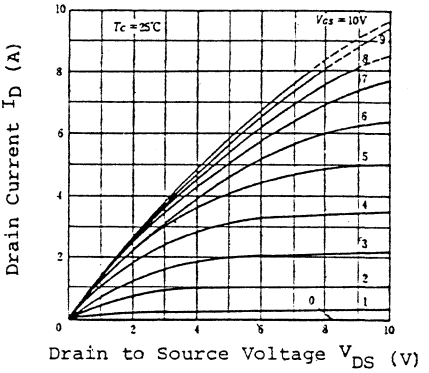
Item	Symbol	Test Condition	2SK175			2SK176			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	I_D=10mA , V_{GS}=-10V	180	-	-	200	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	±20	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=100mA , V_{DS}=10V	0.15	-	1.45	0.15	-	1.45	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=8A , V_{GD}=0	-	-	12	-	-	12	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=10V , I_D=3A	0.7	1.0	1.4	0.7	1.0	1.4	S
Input Capacitance	Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	800	-	-	800	-	PF
Output Capacitance	Coss		-	600	-	-	600	-	PF
Reverce Transfer Capacitance	Crss		-	15	-	-	15	-	PF
Turn on Time	t_{on}	V_{DD}=30V I_D=4A	-	250	-	-	250	-	ns
Turn-off-Time	t_{off}		-	90	-	-	90	-	ns

* Pulse Test

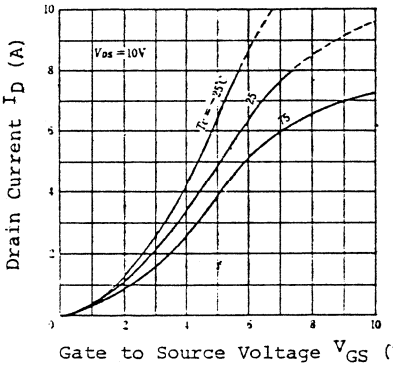
TYPICAL OUTPUT CHARACTERISTICS (1)



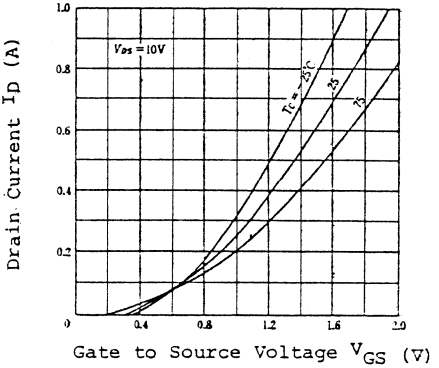
TYPICAL OUTPUT CHARACTERISTICS (2)



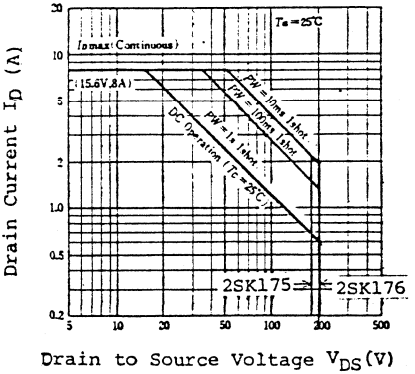
TYPICAL TRANSFER CHARACTERISTICS (1)



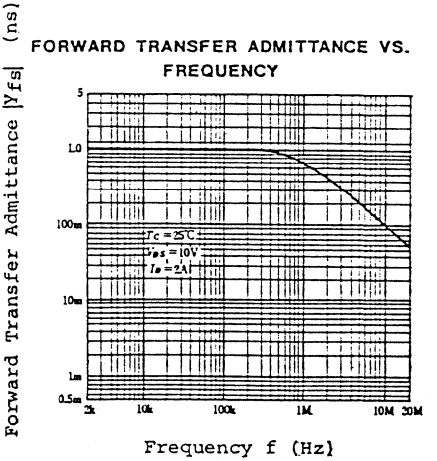
TYPICAL TRANSFER CHARACTERISTICS (2)



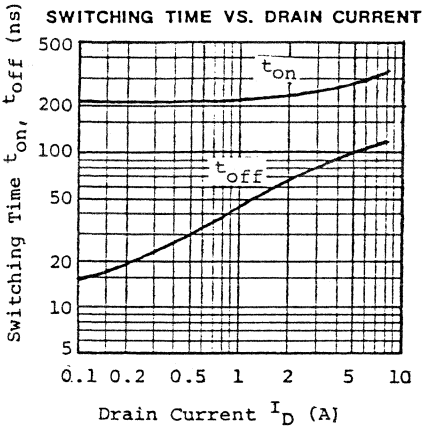
AREA OF SAFE OPERATION



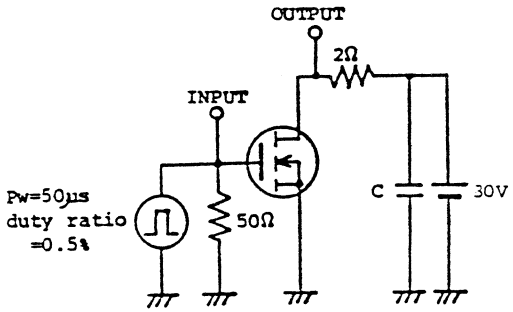
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME VS. DRAIN CURRENT

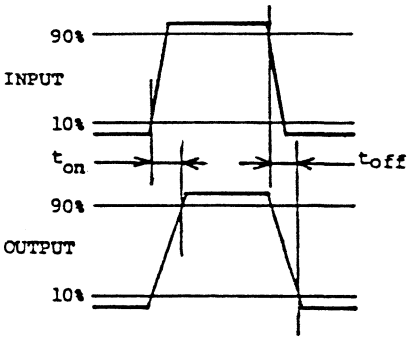


SWITCHING TIME TESTING CIRCUIT



C:bypass capacitor

RESPONSE WAVE FORM

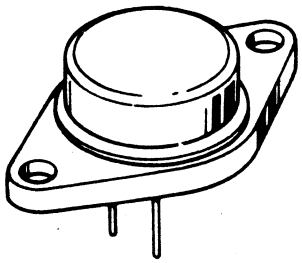


2SK176H
(COMPLEMENT TO 2SJ56H)

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. High Speed Switching.
2. High Cutoff Frequency (f_C=7MHz)
3. Enhancement-Mode
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.



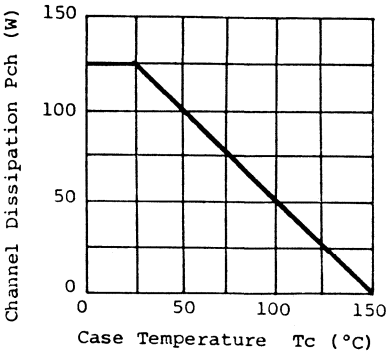
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	200	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Channel Dissipation	Pch*	125	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-65 ~ +150	°C

*Tc=25°C

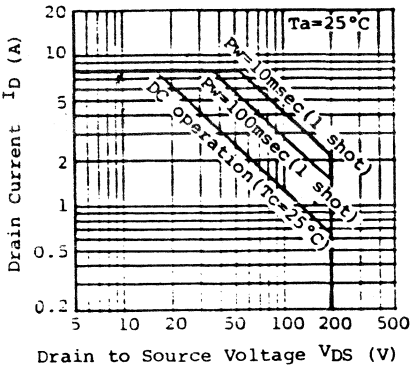
CHANNEL DISSIPATION CURVE



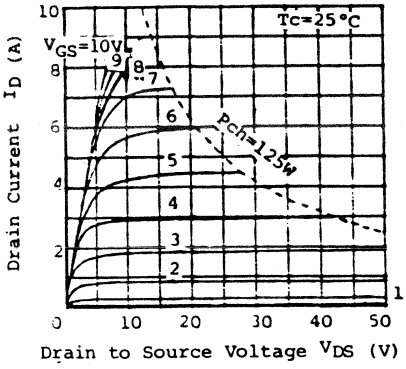
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	200	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.55	-	3.0	V
Drain Current	I_{DSS}	V_{DS}=160V, V_{GS}=0	-	-	3.0	mA
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=4A, V_{GS}=15V	-	-	6.0	V
Foward Transfer Admittance	$\|Yfs\|$	V_{DS}=10V, I_D=3A	0.7	-	1.4	S
Input Capacitance	Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	800	-	pF
Output Capacitance	Coss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	600	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	60	-	ns
Turn off Time	t_{off}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	200	-	ns

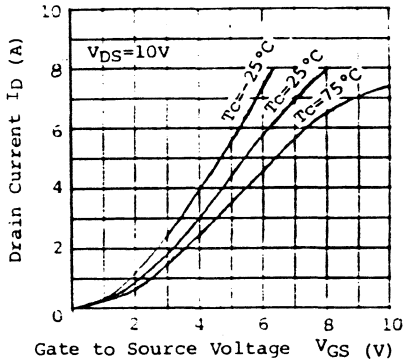
AREA OF SAFE OPERATION



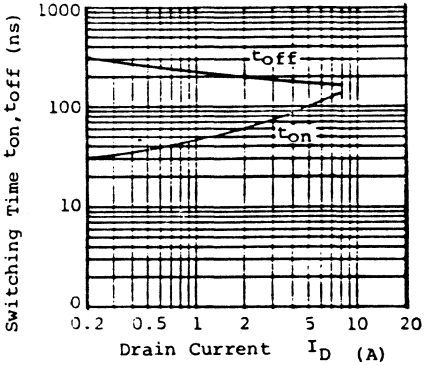
TYPICAL OUTPUT CHARACTERISTICS



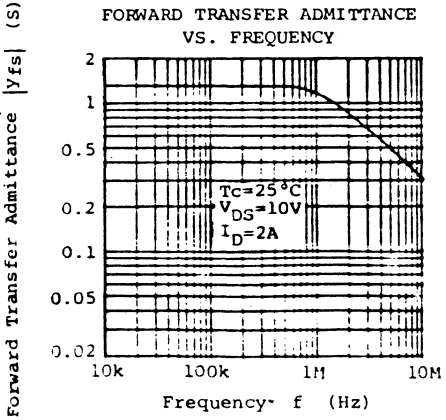
DRAIN CURRENT VS.
GATE TO SOURCE VOLTAGE



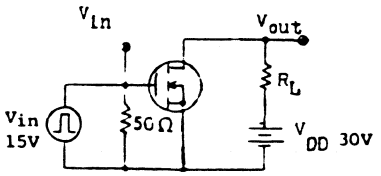
SWITCHING TIME VS. DRAIN CURRENT



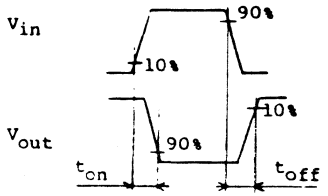
FORWARD TRANSFER ADMITTANCE
VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM

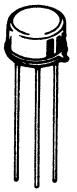


2SK196 H

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. High Speed Switching
2. High Cutoff Frequency (f_c=30MHz)
3. Enhancement-Mode
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.

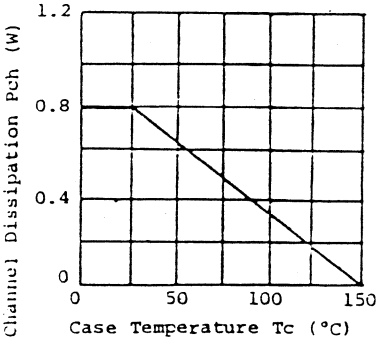


(JEDEC TO-39)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	160	V
Gate to Source Voltage	V_{GSS}	±14	V
Drain Current	I_D	500	mA
Channel Dissipation	Pch	0.8	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-65 ~ +150	°C

CHANNEL DISSIPATION CURVE

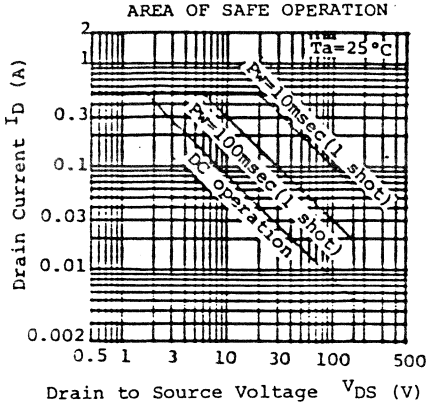


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

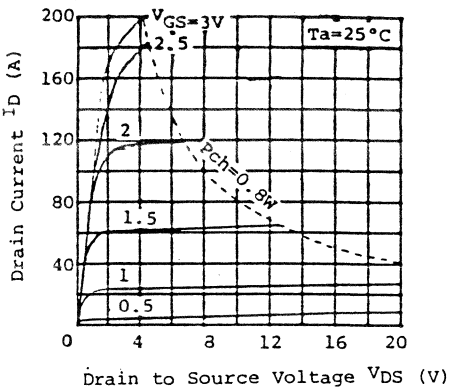
Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	160	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±10μA, V_{DS}=0	±14	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=10mA, V_{DS}=10V	0.2	-	2.0	V
Drain Current	I_{DSS}	V_{DS}=120V, V_{GS}=0	-	-	2.0	mA
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=200mA, V_{GS}=10V	-	-	3.0	V
Foward Transfer Admittance	|Yfs|	V_{DS}=10V, I_D=200mA(pulse)	50	-	-	mS
Input Capacitance	Ciss	V_{DS}=10V, I_D=10mA, f=1MHz	-	90	-	pF
Output Capacitance	Coss	V_{DS}=10V, I_D=10mA, f=1MHz	-	60	-	pF
Turn-on Time	t_{on}	V_{GS}=10V, I_D=200mA, R_L=150Ω	-	20	-	ns
Turn off Time	t_{off}	V_{GS}=10V, I_D=200mA, R_L=150Ω	-	30	-	ns

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

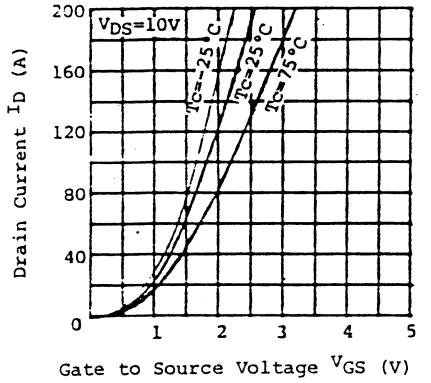
AREA OF SAFE OPERATION



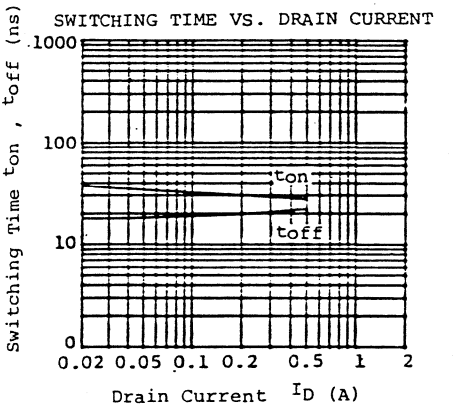
TYPICAL OUTPUT CHARACTERISTICS



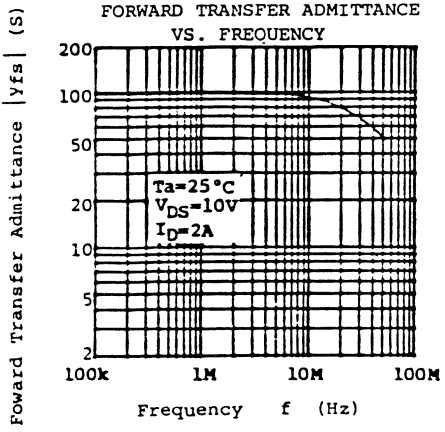
DRAIN CURRENT VS.
GATE TO SOURCE VOLTAGE



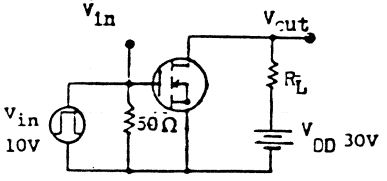
SWITCHING TIME VS. DRAIN CURRENT



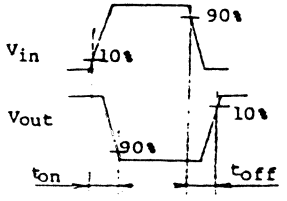
FORWARD TRANSFER ADMITTANCE
VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT

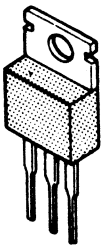


RESPONSE WAVE FORM



2SK213/214/215/216
(COMPLEMENT TO 2SJ76/77/78/79)

SILICON N CHANNEL MOS FET
HIGH FREQUENCY AND LOW FREQUENCY POWER AMPLIFIER, HIGH SPEED POWER SWITCHING



(JEDEC TO-220AB)

Features;

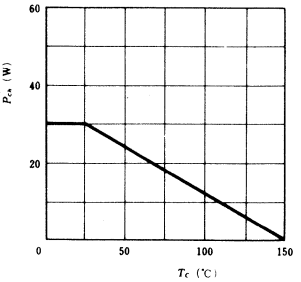
1. Suitable for direct mounting
2. High forward transfer addmittance
3. Excellent frequency response
4. Enhancement-mode

■ ABSOLUTE MAXIMUM RATINGS ($Ta=25°C$)

Item	Symbol		Unit
Drain to Source Voltage	V_{DSX}	200 (2SK216)	V
Gate to Source Voltage	V_{GSS}	± 5	V
Drain Current	I_D	500	mA
Channel Dissipation	P_{ch}	1.75	W
	P_{ch}*	30	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−45 ~ +150	°C

* Value at $T_C=25°C$

MAXIMUM CHANNEL DISSIPATION CURVE

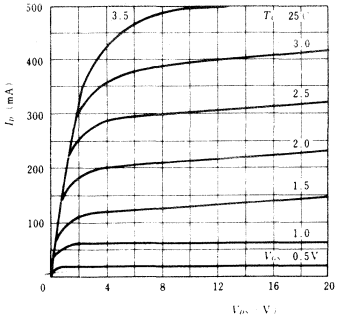


■ ELECTRICAL CHARACTERISTICS ($Ta=25°C$)

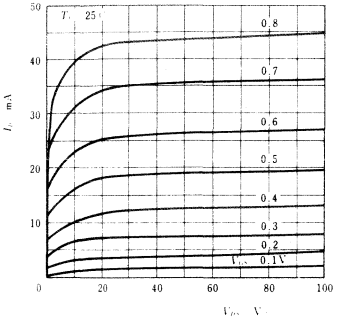
Item		Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	213	$V_{(BR)DSX}$	$V_{GS}=-2V$, $I_D=1mA$	140	−	−	V
	214			160			
	215			180			
	216			200			
Gate to Source Breakdown Voltage		$V_{(BR)GSS}$	$I_G=\pm 10\mu A$, $V_{DS}=0$	±15	−	−	V
Gate to Source Voltage		$V_{GS(on)}$	$V_{DS}=10V$, $I_D=10mA$ *	0.2	−	1.5	V
Drain to Source Saturation Voltage		$V_{DS(sat)}$	$I_D=10mA$, $V_{GD}=0$ *	−	−	2	V
Forward Transfer Admittance		$\|y_{fs}\|$	$V_{DS}=20V$, $I_D=10mA$ *	−	40	−	mS
Input Capacitance		C_{iss}	$V_{DS}=10V$, $I_D=10mA$, $f=1MHz$	−	90	−	pF
Feedback Capacitance		C_{rss}		−	2.2	−	pF

* Pulse Test

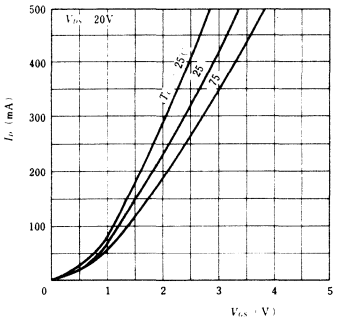
TYPICAL OUTPUT CHARACTERISTICS



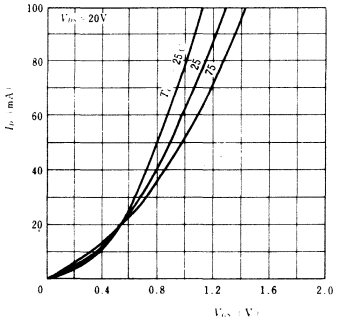
TYPICAL OUTPUT CHARACTERISTICS



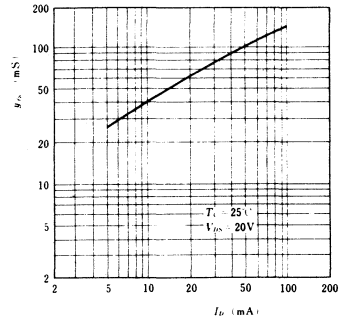
TYPICAL TRANSFER CHARACTERISTICS



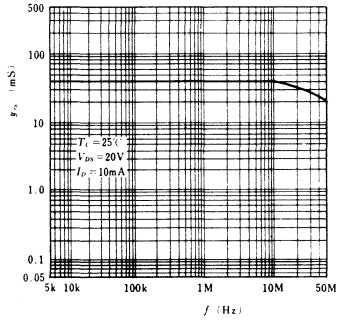
TYPICAL TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



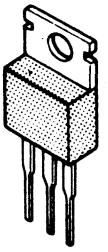
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



2SK214K/216K

(COMPLEMENT TO 2SJ77K/79K

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER
Complementary pair with 2SJ77Ⓚ, 2SJ79Ⓚ



(JEDEC TO-220AB)

Features;

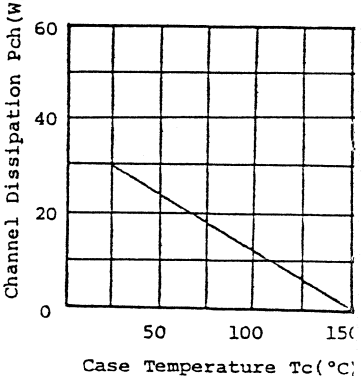
1. High Speed Switching
2. High Cutoff Frequency (f_c=30MHz)
3. High Breakdown Voltage
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating 2SK214Ⓚ	Rating 2SK216Ⓚ	Unit
Drain to Source Voltage	V_{DSX}	160	200	V
Gate to Source Voltage	V_{GSS}	±15	±15	V
Drain Current	I_D	500	500	A
Channel Dissipation	Pch	1.75	1.75	W
	Pch*	30	30	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-45 ~ +150	-45 ~ +150	°C

* Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATIO CURVE

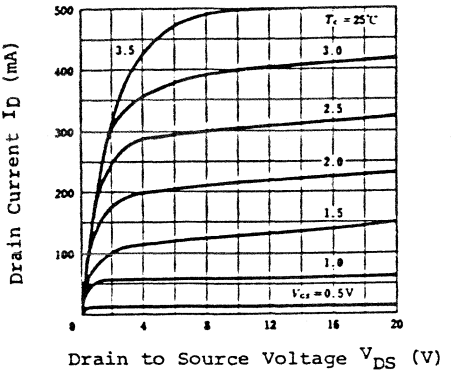


■ ELECTRICAL CHARACTERISTICS (Tc=25°C)

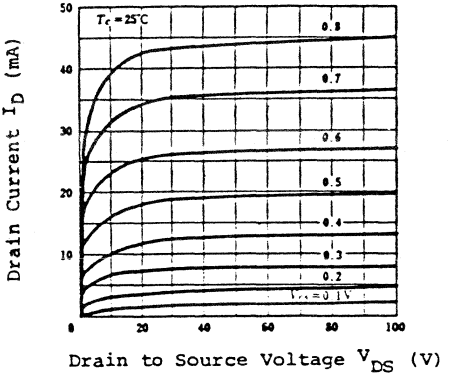
Item	Symbol	Test Condition	2SK214Ⓚ min	2SK214Ⓚ typ	2SK214Ⓚ max	2SK216Ⓚ min	2SK216Ⓚ typ	2SK216Ⓚ max	Uni
Drain to Source Breakdown Voltage	$V_{(BR)DSX}$	V_{GS}=-2V, I_D=1mA	160	-	-	200	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_{GS}=±10μA, V_{DS}=0	±15	-	-	±15	-	-	V
Gate to Source Voltage	$V_{GS(on)}$	V_{DS}=10V, I_D=10mA *	0.2	-	1.5	0.2	-	1.5	V
Drain to Source Saturation Voltage	$V_{DS(sat)}$	I_D=10mA, V_{GD}=0 *	-	-	2.0	-	-	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=20V, I_D=10mA *	-	40	-	-	40	-	S
Input Capacitance	Ciss	V_{DS}=10V, I_D=10mA f=1MHz	-	90	-	-	90	-	Pl
Output Capacitance	Crss		-	2.2	-	-	2.2	-	Pl

* Pulse Test.

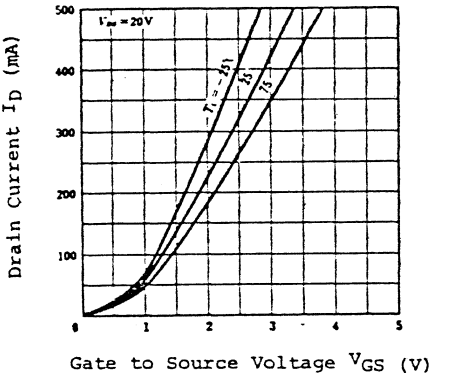
TYPICAL OUTPUT CHARACTERISTICS (1)



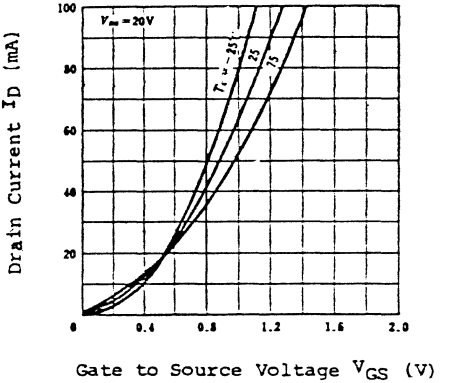
TYPICAL OUTPUT CHARACTERISTICS (2)



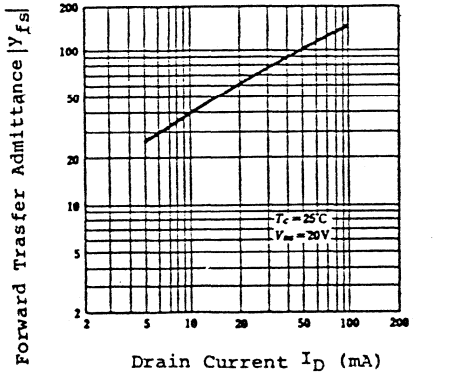
TYPICAL TRANSFER CHARACTERISTICS (1)



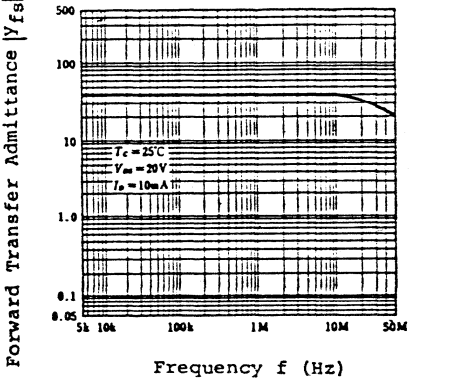
TYPICAL TRANSFER CHARACTERISTICS (2)



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



FORWARD TRANSFER ADMITTANCE VS. FREQUENCY

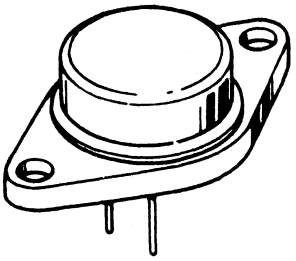


2SK220H/221H

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. High Speed Switching
2. High Cutoff Frequency (f_C=50MHz)
3. Enhancement-Mode
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.



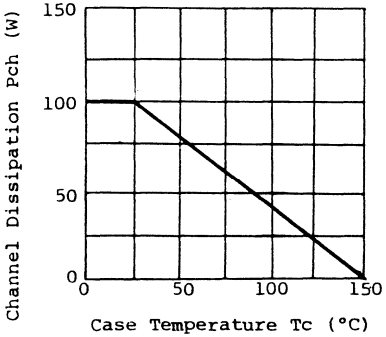
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	200(2SK221)	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Channel Dissipation	Pch*	100	W
Storage Temperature	T_{stg}	-65~+150	°C

*Tc=25°C

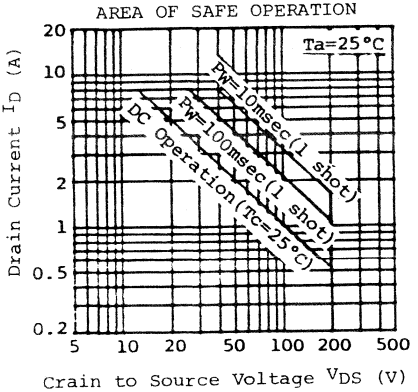
CHANNEL DISSIPATION CURVE



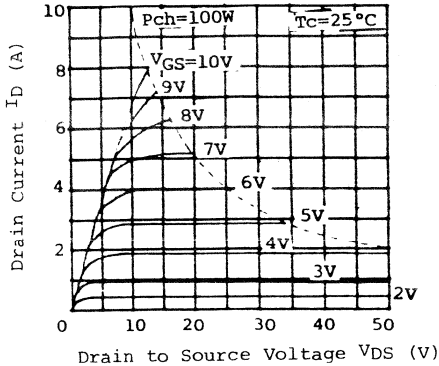
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	2SK220H	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	160	-	-	V
	2SK221H			200	-	-	
Gate to Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate to Source Cutoff Voltage		$V_{GS(off)}$	I_D=10mA, V_{DS}=10V	0.4	-	3.0	V
Drain Current		I_{DSS}	V_{DS}=160V, V_{GS}=0	-	-	1.0	mA
Drain to Source Saturation Voltage		$V_{DS(ON)}$	I_D=4A, V_{GS}=15V	-	-	6.0	V
Foward Transfer Admittance		|Yfs|	V_{DS}=10V, I_D=3A	0.6	0.9	-	S
Input Capacitance		Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	600	-	pF
Output Capacitance		Coss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	300	-	pF
Turn on Time		t_{on}	I_D=2A, V_{GS}=15V	-	25	-	ns
Turn off Time		t_{off}	I_D=2A, V_{GS}=15V	-	45	-	ns

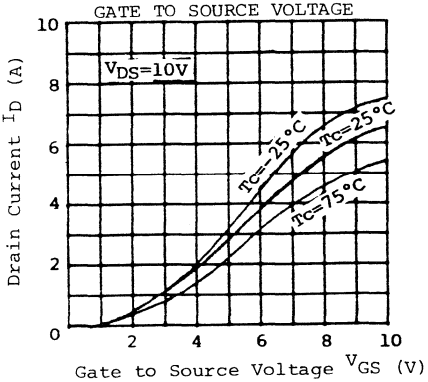
AREA OF SAFE OPERATION



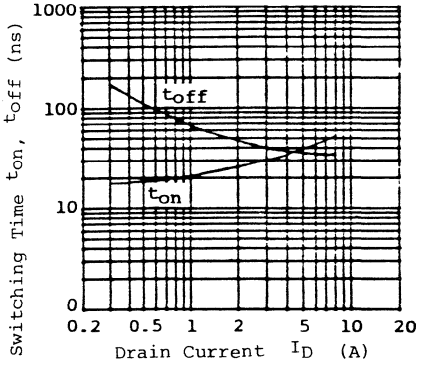
TYPICAL OUTPUT CHARACTERISTICS



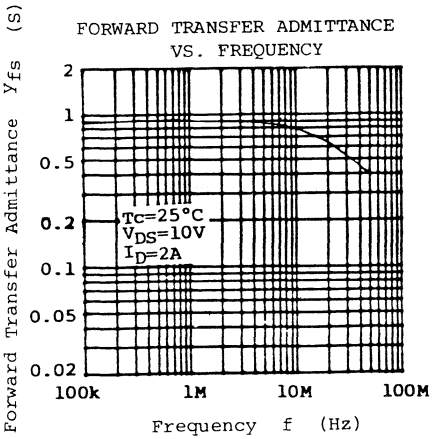
DRAIN CURRENT VS.
GATE TO SOURCE VOLTAGE



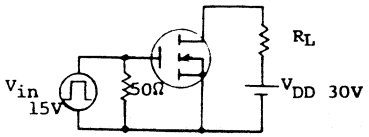
SWITCHING TIME VS. DRAIN CURRENT



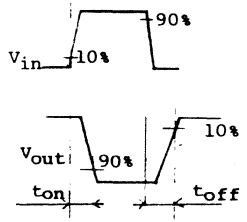
FORWARD TRANSFER ADMITTANCE
VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM



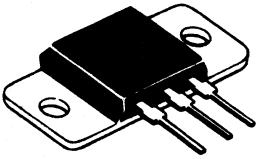
2SK225/226/227

COMPLEMENT TO 2SJ81/82/83)

SILICON N-CHANNEL MOS FET
LOW FREQUENCY POWER AMPLIFIER

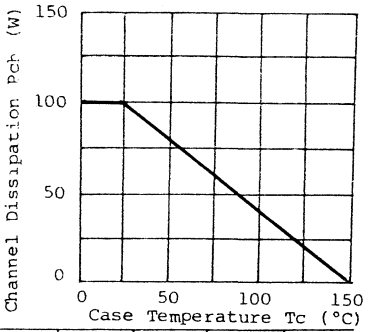
Features;

1. High Power Gain.
2. Excellent Frequency Response.
3. High Speed Switching.
4. Wide Area of Safe Operation.
5. Enhancement-mode.
6. Good Complementary Characteristics.
7. Equipped with Gate Protection Diodes.



(HPAK)

MAXIMUM CHANNEL DISSIPATION CURV



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSX}	160(2SK227)	V
Gate to Source Voltage	V_{GSS}	±15	V
Drain Current	I_D	7	A
Channel Dissipation	Pch*	100	W
Storage Temperature	T_{stg}	-45~+150	°C

*Tc=25°C

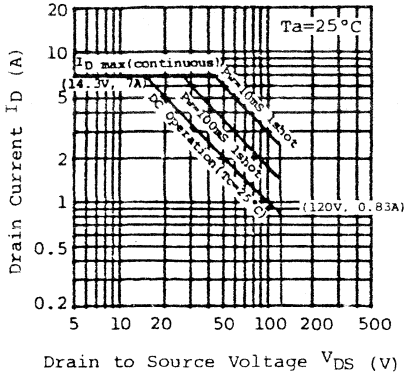
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item		Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	2SK225	$V_{(BR)DSX}$	I_D=10mA, V_{GS}=-10V	120	-	-	V
	2SK226			140	-	-	
	2SK227			160		-	
Gate to Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±15	-	-	V
Gate to Source Cutoff Voltage		$V_{GS(off)}$	I_D=100mA, V_{DS}=10V	0.15	-	1.45	V
Drain to Source Saturation Voltage		$V_{DS(sat)}$	I_D=7A, V_{GD}=0 *	-	-	12	V
Forward Transfer Admittance		$\|y_{fs}\|$	V_{DS}=10V, I_D=3A *	0.7	1.0	1.4	S
Input Capacitance		Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	600	-	pF
Output Capacitance		Coss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	350	-	pF
Reverse Transfer Capacitance		Crss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	10	-	pF
Turn on Time		t_{on}	V_{DD}=20V, I_D=4A	-	180	-	ns
Turn off Time		t_{off}		-	60	-	ns

*Pulse Test

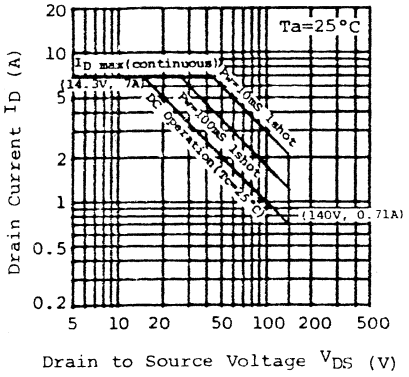
2SK225

AREA OF SAFE OPERATION



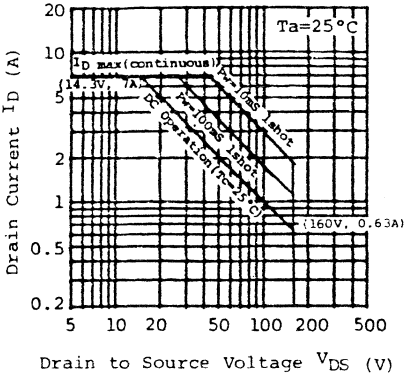
2SK226

AREA OF SAFE OPERATION

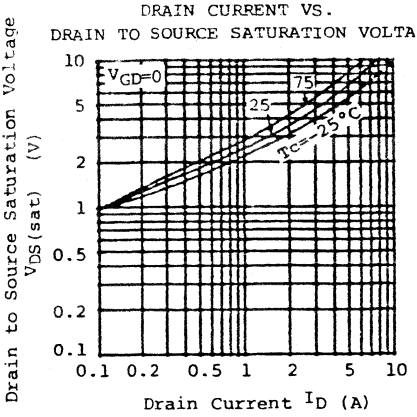


2SK227

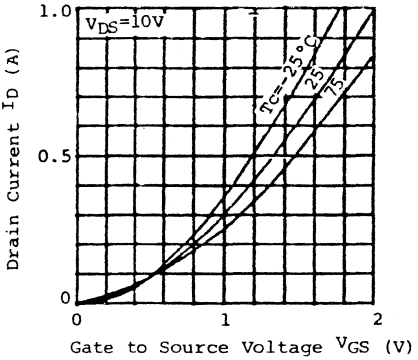
AREA OF SAFE OPERATION



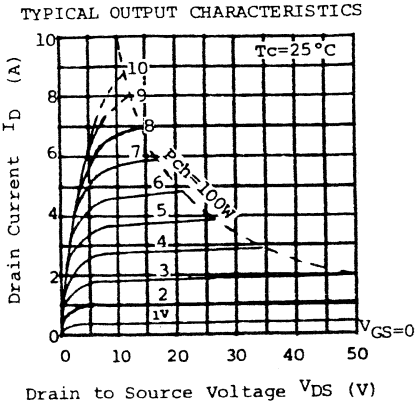
DRAIN CURRENT VS.
DRAIN TO SOURCE SATURATION VOLTAGE



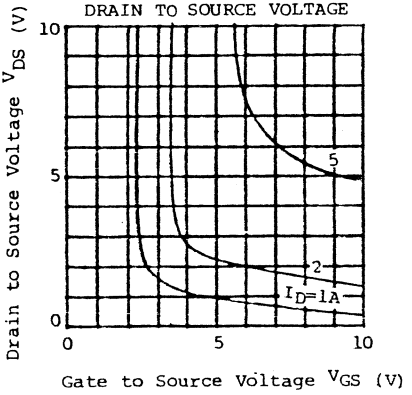
TYPICAL TRANSFER CHARACTERISTICS



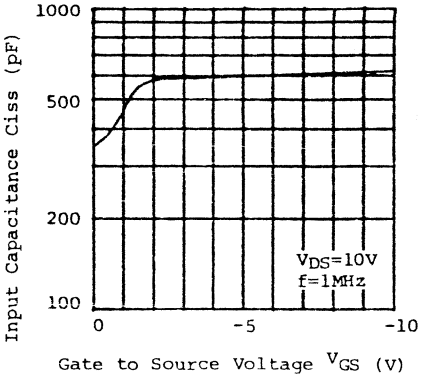
TYPICAL OUTPUT CHARACTERISTICS



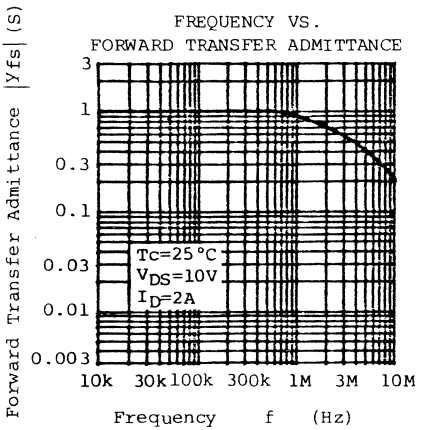
GATE TO SOURCE VOLTAGE VS.
DRAIN TO SOURCE VOLTAGE



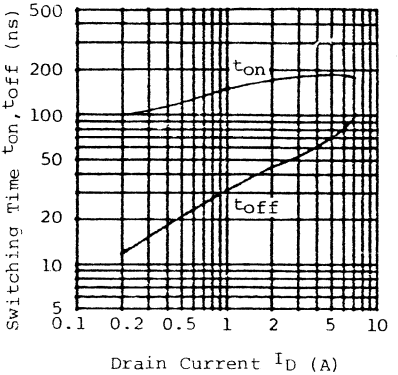
GATE TO SOURCE VOLTAGE VS.
INPUT CAPACITANCE



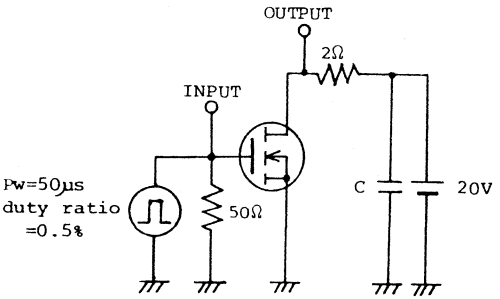
FREQUENCY VS.
FORWARD TRANSFER ADMITTANCE



DRAIN CURRENT VS.
SWITCHING TIME

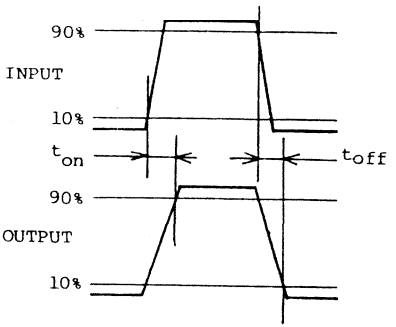


SWITCHING TIME TESTING CIRCUIT



C:bypass capacitor

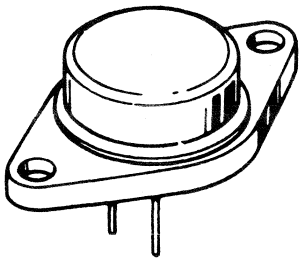
RESPONSE WAVE FORM



SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. High Speed Switching
2. High Cutoff Frequency (f_c=7MHz)
3. Enhancement-Mode
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.

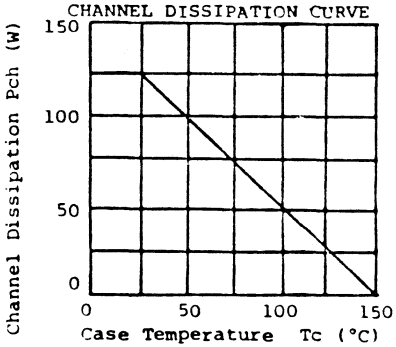


(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	250	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Channel Dissipation	Pch*	125	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-65～+150	°C

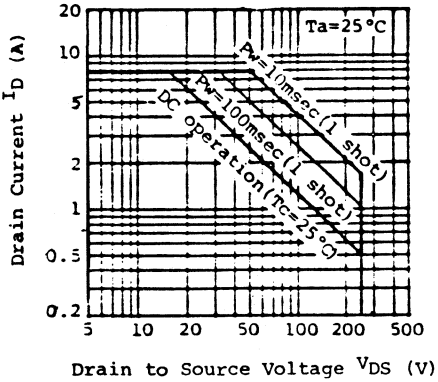
*Tc=25°C



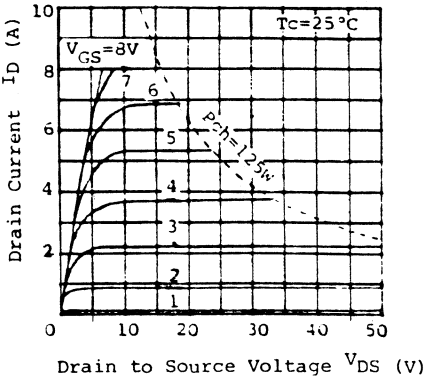
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	250	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=10mA, V_{DS}=10V	0.4	-	3.0	V
Drain Current	I_{DSS}	V_{DS}=200V, V_{GS}=0	-	-	1.0	mA
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=4A, V_{GS}=15V	-	-	4.5	V
Foward Transfer Admittance	|Yfs|	V_{DS}=10V, I_D=3A	0.9	1.3	-	S
Input Capacitance	Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	800	-	pF
Output Capacitance	Coss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	350	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V	-	25	-	ns
Turn off Time	t_{off}	I_D=2A, V_{GS}=15V	-	140	-	ns

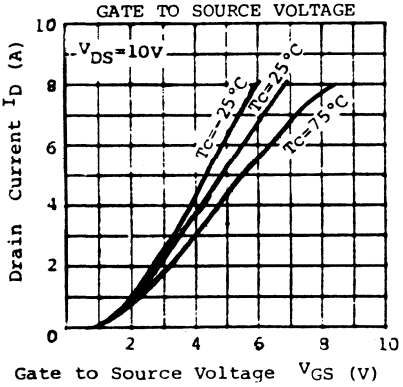
AREA OF SAFE OPERATION



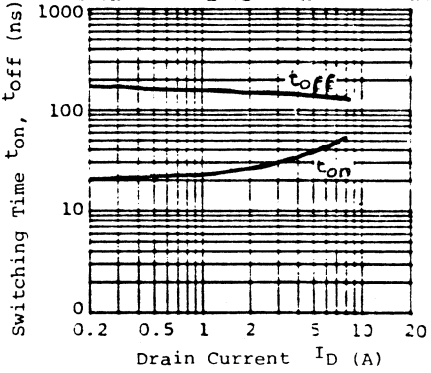
TYPICAL OUTPUT CHARACTERISTICS



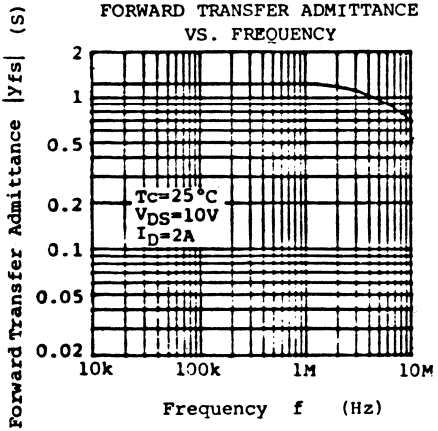
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



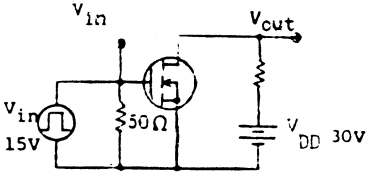
SWITCHING TIME VS. DRAIN CURRENT



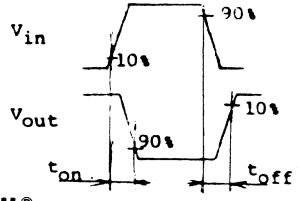
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM

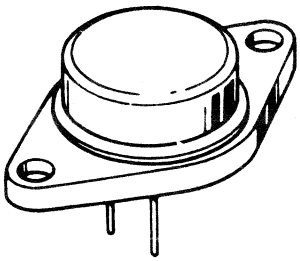


2SK259H/260H

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. High Speed Switching
2. High Cutoff Frequency
3. High Breakdown Voltage
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultransonic Power Oscillators.
5. Enhancement-Mode



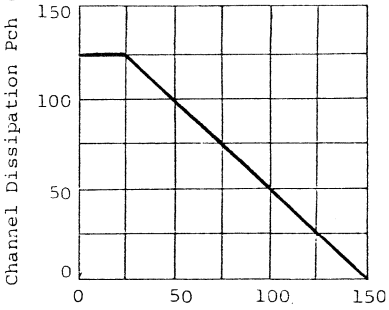
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	400(2SK260)	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(peak)}$	10	A
Channel Dissipation	Pch*	125	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-65～+150	°C

*Tc=25°C

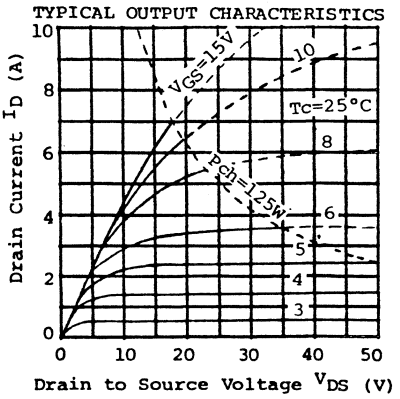
CHANNEL DISSIPATION CURVE



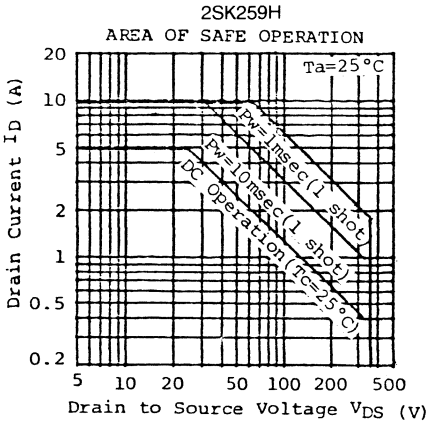
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

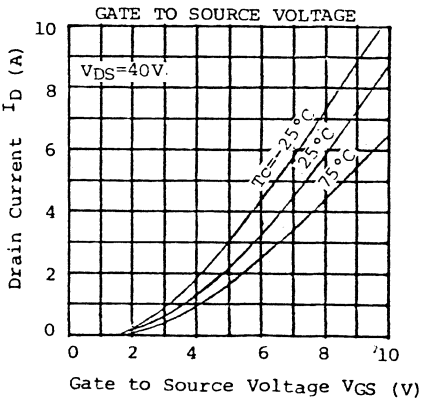
Item		Symbol	Test Condition	min	typ	max	Unit
Drain to Source Breakdown Voltage	2SK259H	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	350	-	-	V
	2SK260H			400	-	-	
Gate to Source Breakdown Voltage		$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate to Source Cutoff Current		$V_{GS(off)}$	I_D=10mA, V_{DS}=10V	0.4	-	3.0	V
Drain Current		I_{DSS}	V_{DS}=280V, V_{GS}=0	-	-	1.0	mA
Drain to Source Saturation Voltage		$V_{DS(ON)}$	I_D=3A, V_{GS}=15V	-	7.5	9.0	V
Foward Transfer Admittance		$\|yfs\|$	V_{DS}=20V, I_D=3A	0.6	1.0	-	S
Input Capacitance		Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	800	-	pF
Output Capacitance		Coss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	350	-	pF
Feedback Capacitance		Crss	V_{GD}=-5V, f=1MHz	-	15	-	pF
Turn on Time		t_{on}	I_D=2A, V_{GS}=15V	-	25	-	ns
Turn off Time		t_{off}	I_D=2A, V_{GS}=15V	-	140	-	ns

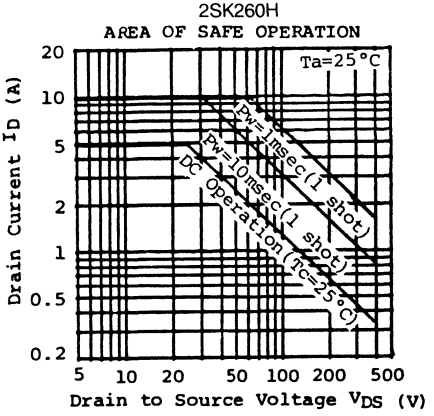
GENERAL CHARACTERISTICS

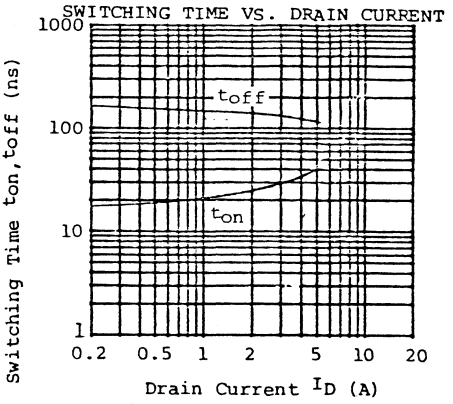


A.S.O. CHARACTERISTICS

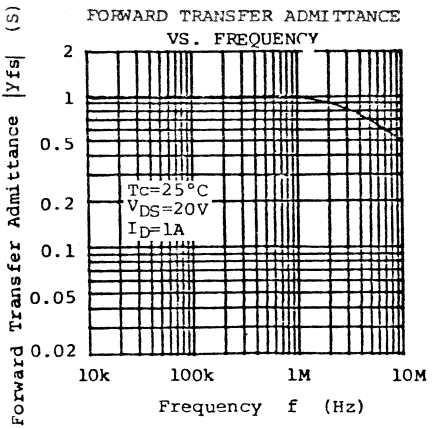




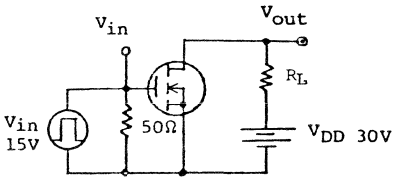




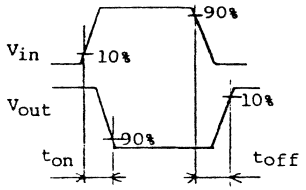
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



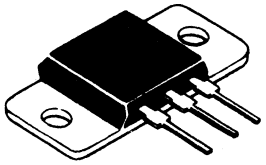
RESPONSE WAVE FORM



2SK286

(COMPLEMENT TO 2SJ96)

SINICON N-CHANNEL ENHANCEMENT-MODE MOS FET
LOW FREQUENCY·HIGH FREQUENCY POWER AMPLIFIER,
HIGH SPEED POWER SWITCHING



(HPAK)

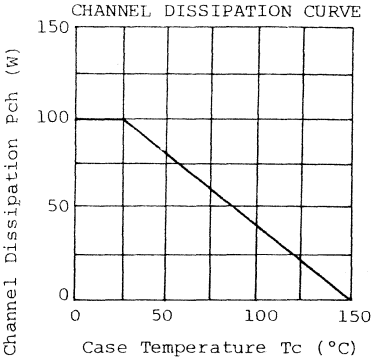
Features;

1. Low Saturation Voltage.(0.5Ω typ)
2. Excellent Frequency Response.
3. High Speed Switching.
4. High Mutual Condactance.
5. Excellent Complementary Characteristics.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSX}	60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Channel Dissipation	Pch*	100	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-45～+150	°C

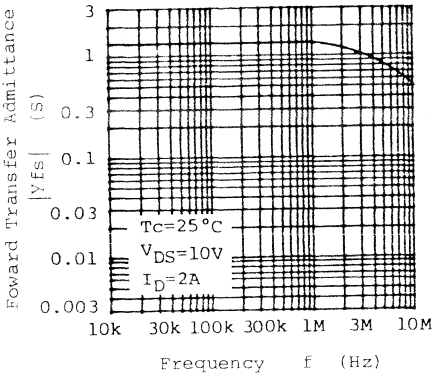
*Tc=25°C



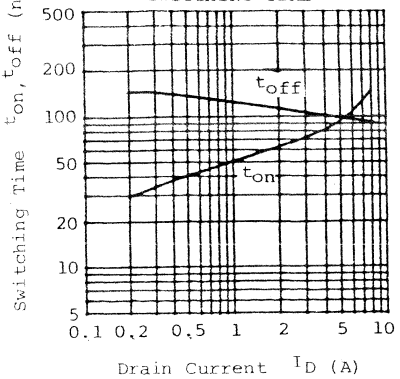
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Drain to Source Cutoff Current	I_{DSX}	V_{DS}=60V, V_{GS}=-10V	-	-	1	mA
Gate to Source Cutoff Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	±1	uA
Gate to Source Cotoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=10mA	0.2	-	1.5	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	V_{GS}=15V, I_D=5A	-	2.5	4.0	V
Foward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=10V, I_D=3A	1.0	1.4	2.5	S
Turn on Time	ton	V_{GS}=10V, I_D=4A	-	80	-	ns
Turn off Time	toff	V_{GS}=10V, I_D=4A	-	110	-	ns
Input Capacitance	Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	500	-	pF

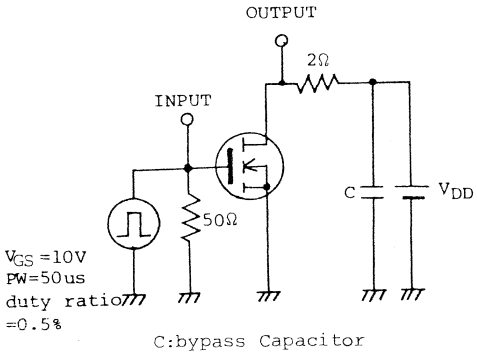
FREQUENCY VS.
FOWARD TRANSFER ADMITTANCE



DRAIN CURRENT VS.
SWITCHING TIME

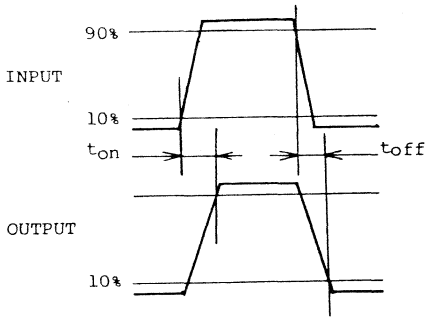


SWITCHING TIME TESTING CIRCUIT

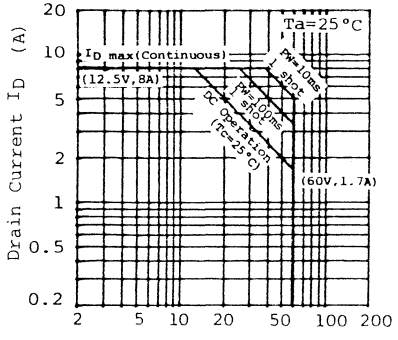


C:bypass Capacitor

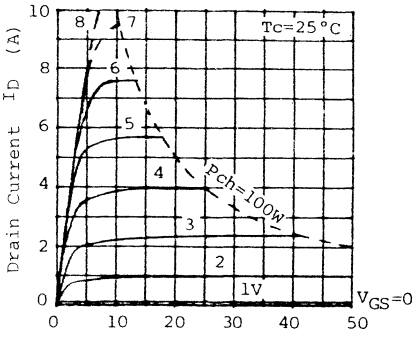
RESPONSE WAVE FORM



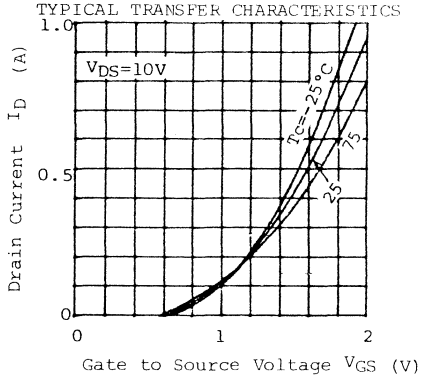
AREA OF SAFE OPERATION



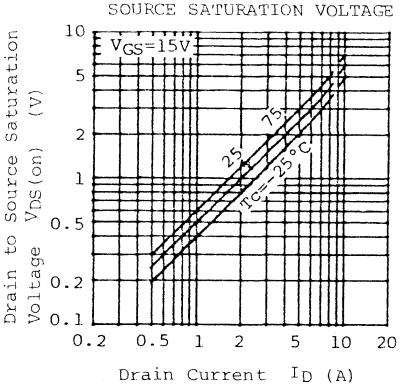
TYPICAL OUTPUT CHARACTERISTICS



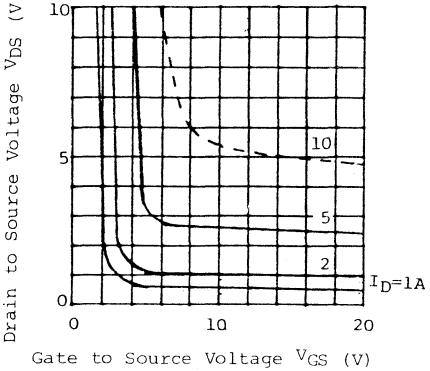
TYPICAL TRANSFER CHARACTERISTICS



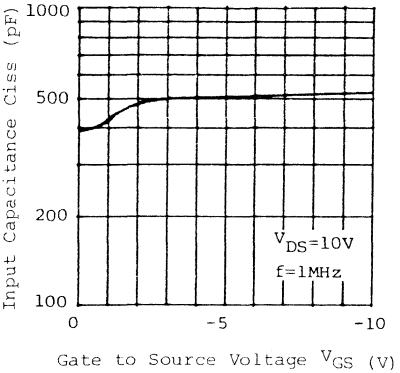
DRAIN CURRENT VS. DRAIN TO SOURCE SATURATION VOLTAGE



GATE TO SOURCE VOLTAGE VS. DRAIN TO SOURCE VOLTAGE



GATE TO SOURCE VOLTAGE VS. INPUT CAPACITANCE

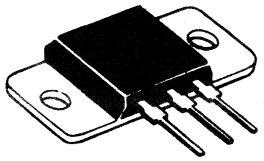


2SK287K/288K

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. High Speed Switching.
2. High Cutoff Frequency.
3. Enhancement-Mode.
4. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



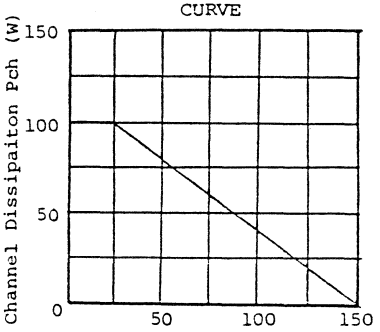
(HPAK)

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating		Unit
		2SK287Ⓚ	2SK288Ⓚ	
Drain to Source Voltage	V_{DSS}	60	80	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	8	8	A
Drain Peak Current	$I_{D(peak)}$	12	12	A
Channel Dissipaiton	Pch*	100	100	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-55～+150	-55～+150	°C

*Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE



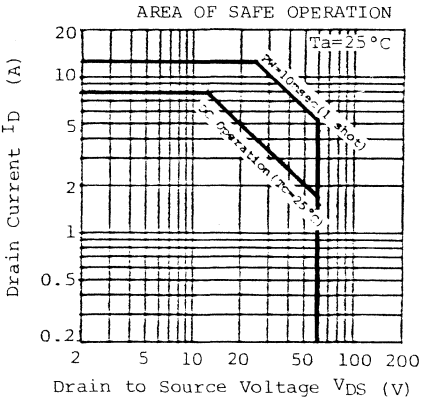
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	2SK287Ⓚ			2SK288Ⓚ			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	60	-	-	80	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	±20	-	-	V
Drain Current	I_{DSS}	2SK287Ⓚ V_{DS}=50V, V_{GS}=0	-	-	1.0	-	-	-	mA
		2SK288Ⓚ V_{DS}=60V, V_{GS}=0	-	-	-	-	-	1.0	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=10mA, V_{DS}=10V	0.4	-	3.0	0.4	-	3.0	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	I_D=5A, V_{GS}=15V *	-	2.5	3.0	-	2.5	3.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=10V, I_D=3A *	1.0	1.4	-	1.0	1.4	-	S
Input Capacitance	Ciss	V_{GS}=-5V, V_{DS}=10V, f=1MHz	-	500	-	-	500	-	pF
Output Capacitance	Coss		-	400	-	-	400	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V	-	25	-	-	25	-	ns
Turn off Time	t_{off}		-	350	-	-	350	-	ns

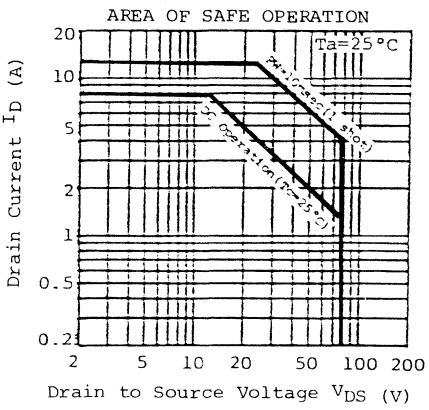
*Pulse Test

A.S.O. CHARACTERISTICS

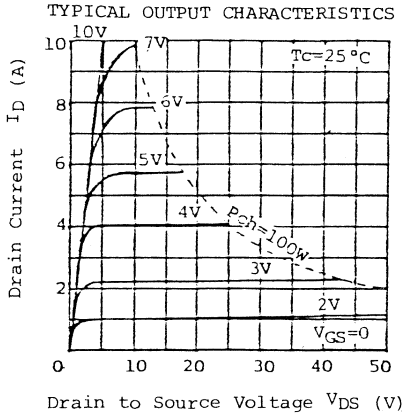
2SK287K

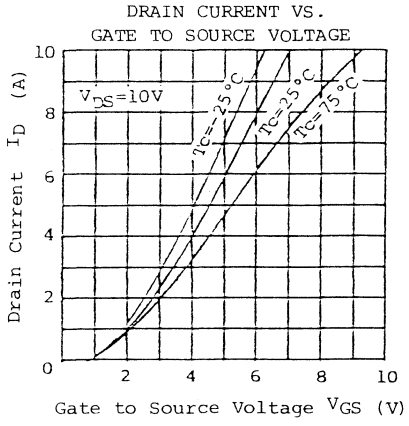


2SK288K

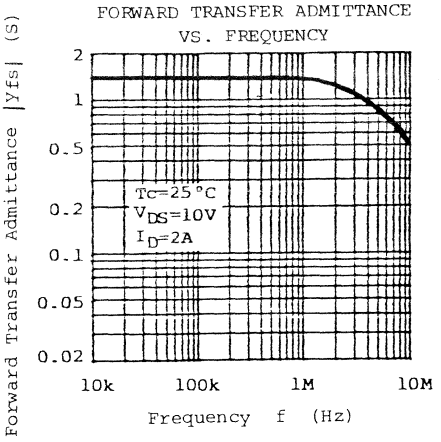


GENERAL CHARACTERISTICS

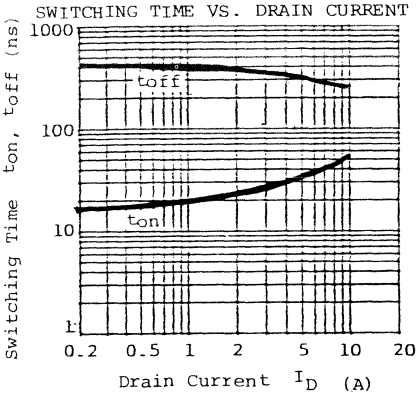




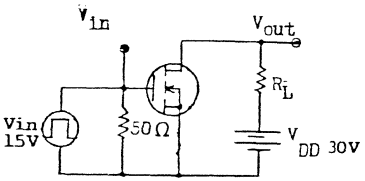
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



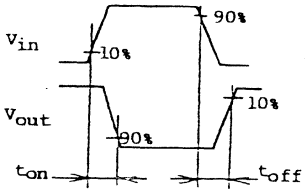
SWITCHING TIME VS. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM

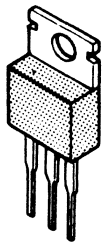


2SK294/295

SILICON N CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. Low On-Resistance.
2. High Speed Switching.
3. High Cutoff Frequency.
4. No Secondary Breakdown.
5. Suitable for Switching Resulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillatcrs.



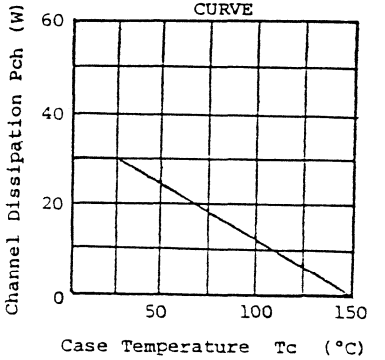
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating		Unit
		2SK294	2SK295	
Drain to Source Voltage	V_{DSS}	80	100	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	5	5	A
Drain Peak Current	$I_{D(peak)}$	10	10	A
Channel Dissipation	Pch*	30	30	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	Tstg	-55~+150	-55~+150	°C

*Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE



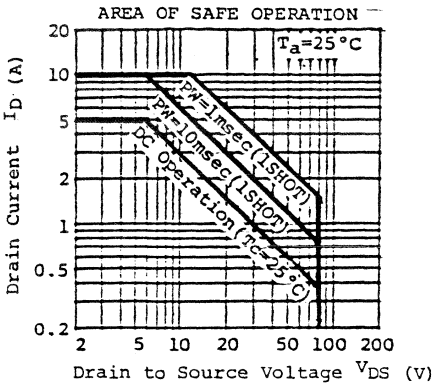
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	2SK294			2SK295			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	80	-	-	100	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	-	-	1	μA
Drain Current	I_{DSS}	K294 V_{DS}=65V, V_{GS}=0	-	-	1	-	-	-	mA
		K295 V_{DS}=80V, V_{GS}=0	-	-	-	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	5.0	1.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	I_D=3A, V_{GS}=15V	-	1.2	1.7	-	1.2	1.7	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=10V	0.5	0.8	-	0.5	0.8	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	450	-	-	450	-	pF
Output Capacitance	Coss		-	270	-	-	270	-	pF
Reverce Transfer Capacitance	Crss		-	140	-	-	140	-	pF
Turn on Time	ton	I_D=2A, V_{GS}=15V, R_L=15Ω	-	40	-	-	40	-	ns
Turn off Time	toff		-	70	-	-	70	-	ns

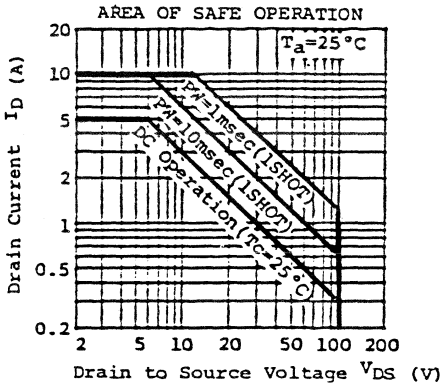
*Pulse Test

A.S.O. CHARACTERISTICS

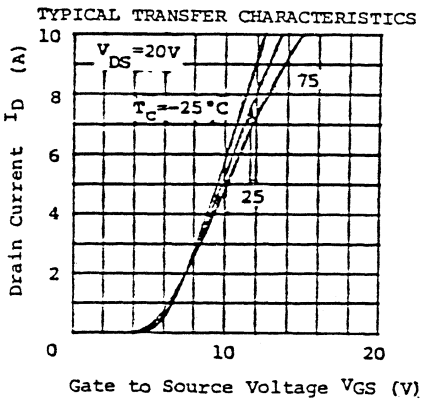
2SK294

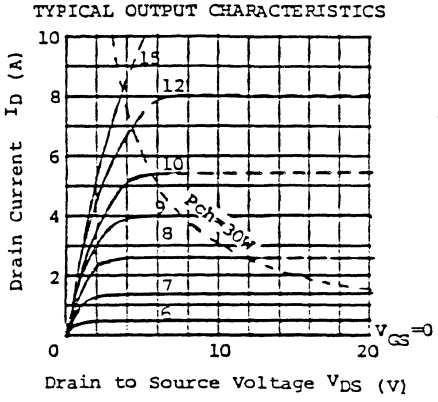


2SK295

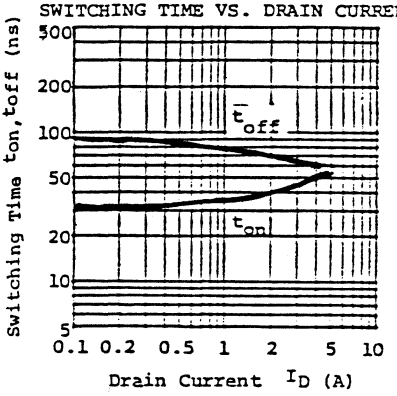


GENERAL CHARACTERISTICS

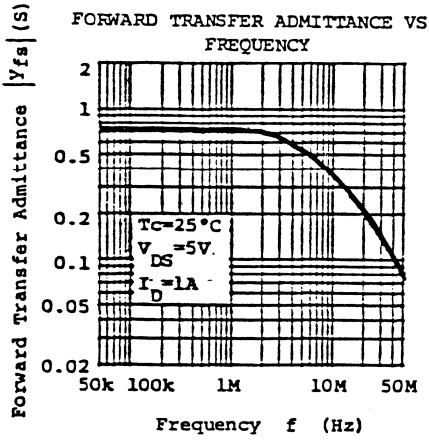




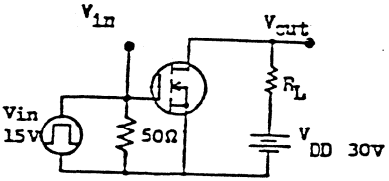
SWITCHING TIME VS. DRAIN CURRENT



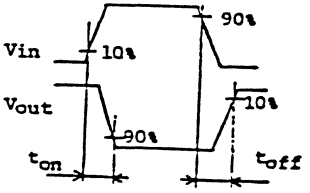
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM



2SK296

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

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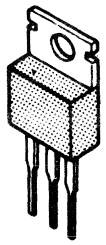


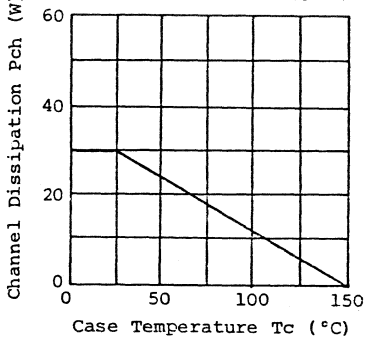
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	300	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	1	A
Drain Peak Current	$I_{D(peak)}$	2	A
Channel Dissipation	Pch*	30	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

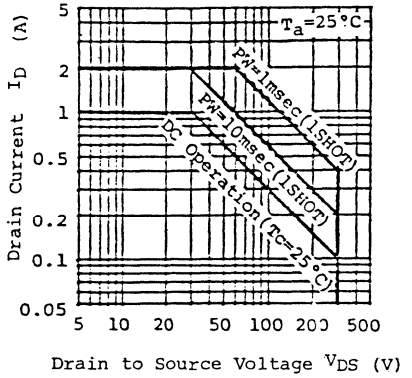
CHANNEL DISSIPATION CURVE



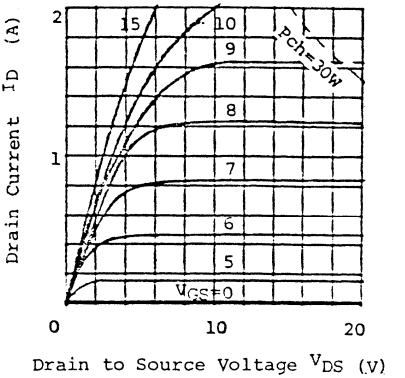
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	300	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=240V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	0.4	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=1A, V_{GS}=15V	-	2.5	4.0	V
Foward Transfer Admittance	Yfs	I_D=0.5A, V_{DS}=10V	0.2	0.4	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	140	-	pF
Output Capacitance	Coss	"	-	65	-	pF
Reverse Transfer Capacitance	Crss	"	-	23	-	pF
Turn on Time	t_{on}	I_D=0.5A, V_{GS}=15V, R_L=60Ω	-	20	-	ns
Turn off Time	t_{off}	"	-	70	-	ns

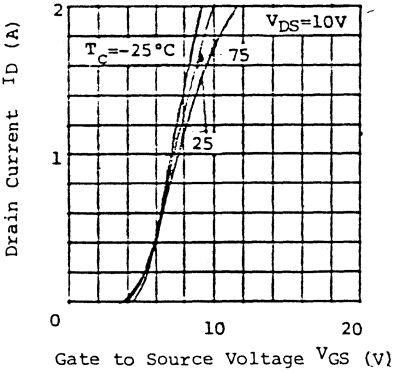
AREA OF SAFE OPERATION



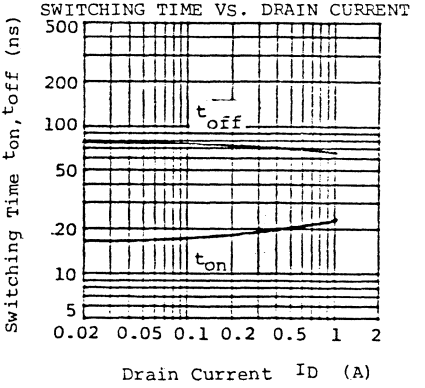
TYPICAL OUTPUT CHARACTERISTICS



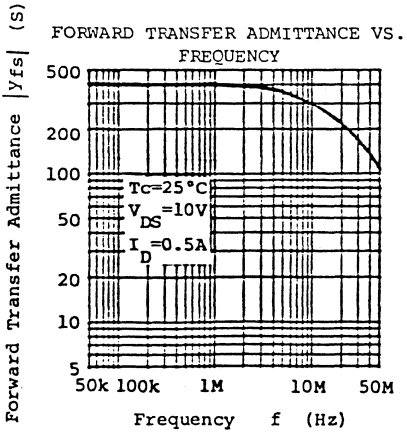
TYPICAL TRANSFER CHARACTERISTICS



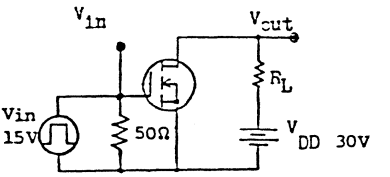
SWITCHING TIME VS. DRAIN CURRENT



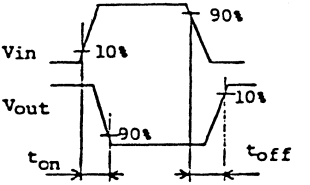
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM



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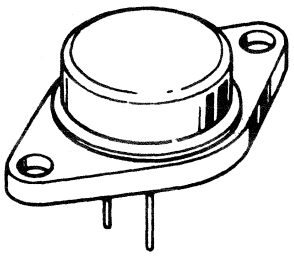


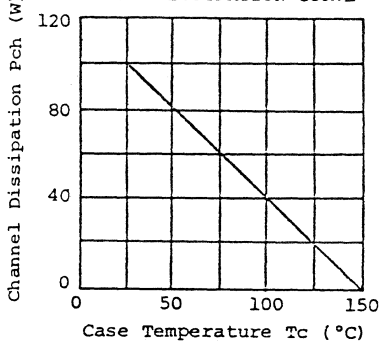
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	400	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Drain Peak Current	$I_{D(peak)}$	12	A
Channel Dissipation	Pch*	100	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

CHANNEL DISSIPATION CURVE

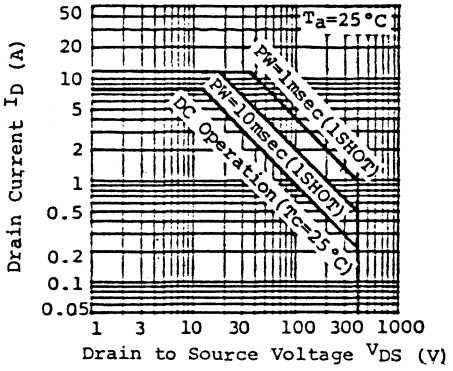


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

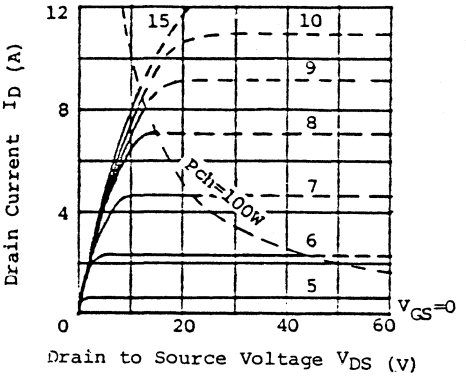
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=320V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=4A, V_{GS}=15V	-	4.4	6.0	V
Foward Transfer Admittance	$\|Yfs\|$	I_D=4A, V_{DS}=10V	1.2	1.7	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	800	-	pF
Output Capacitance	Coss	"	-	180	-	pF
Reverse Transfer Capacitance	Crss	"	-	20	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	50	-	ns
Turn off Time	t_{off}	"	-	120	-	ns

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

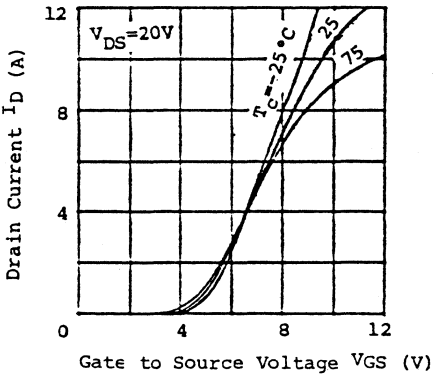
AREA OF SAFE OPERATION



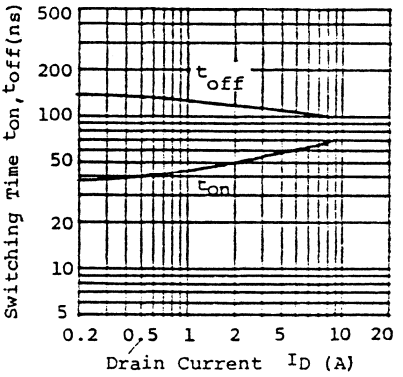
TYPICAL OUTPUT CHARACTERISTICS



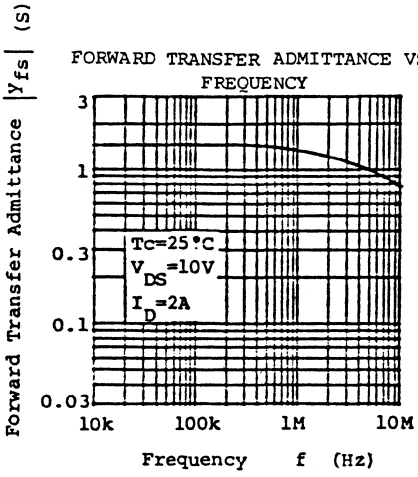
TYPICAL TRANSFER CHARACTERISTICS



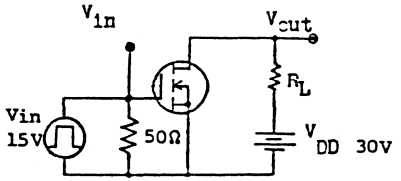
SWITCHING TIME VS. DRAIN CURRENT



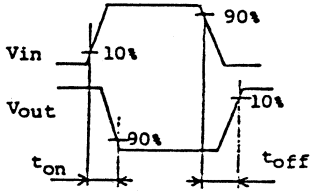
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM



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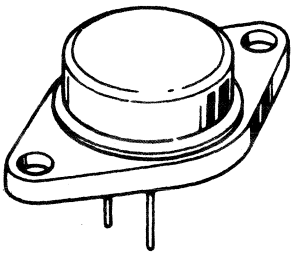


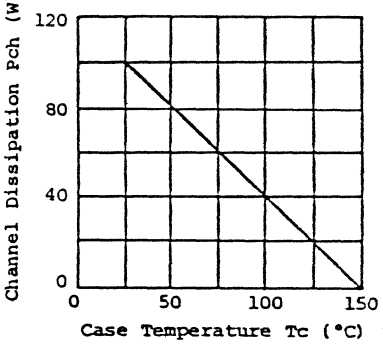
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	450	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Drain Peak Current	$I_{D(peak)}$	12	A
Channel Dissipation	Pch*	100	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

CHANNEL DISSIPATION CURVE

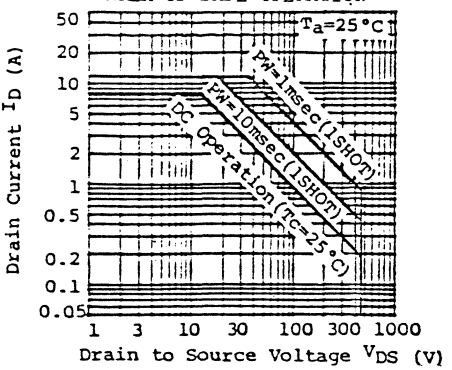


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

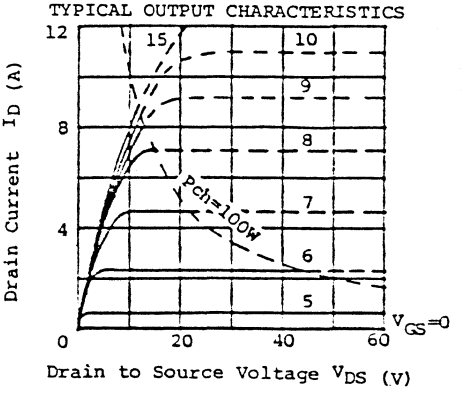
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=4A, V_{GS}=15V	-	4.4	6.0	V
Foward Transfer Admittance	$\|Yfs\|$	I_D=4A, V_{DS}=10V	1.2	1.7	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	800	-	pF
Output Capacitance	Coss	"	-	180	-	pF
Reverse Transfer Capacitance	Crss	"	-	20	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	50	-	ns
Turn off Time	t_{off}	"	-	120	-	ns

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

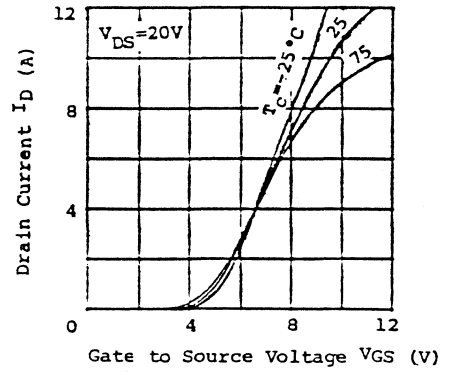
AREA OF SAFE OPERATION



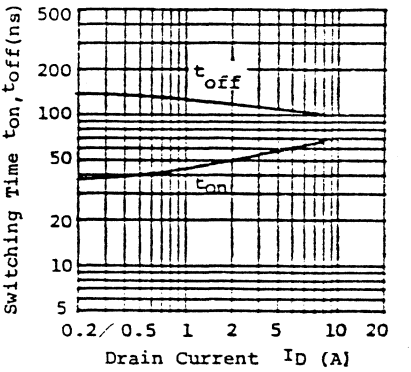
TYPICAL OUTPUT CHARACTERISTICS



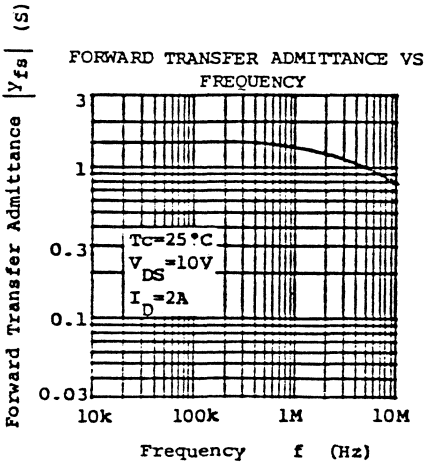
TYPICAL TRANSFER CHARACTERISTICS



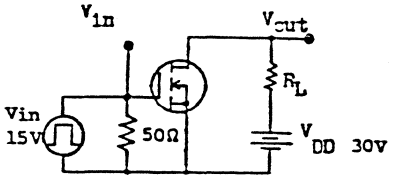
SWITCHING TIME VS. DRAIN CURRENT



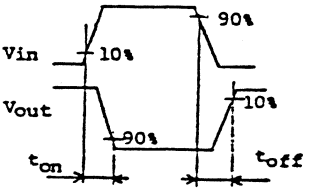
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM



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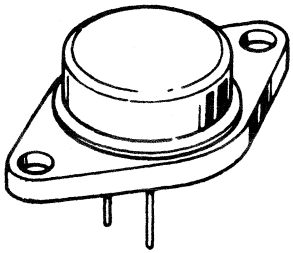


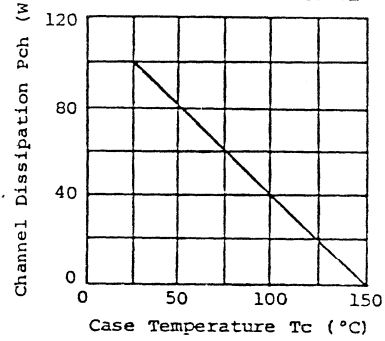
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	120	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	10	A
Drain Peak Current	$I_{D(peak)}$	15	A
Channel Dissipation	Pch*	100	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

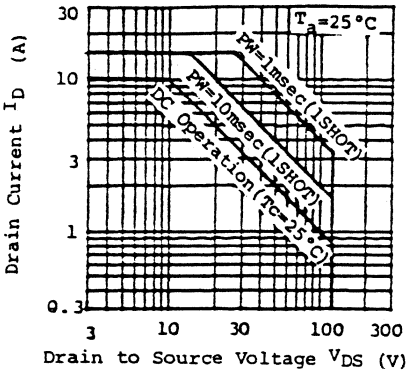
CHANNEL DISSIPATION CURVE



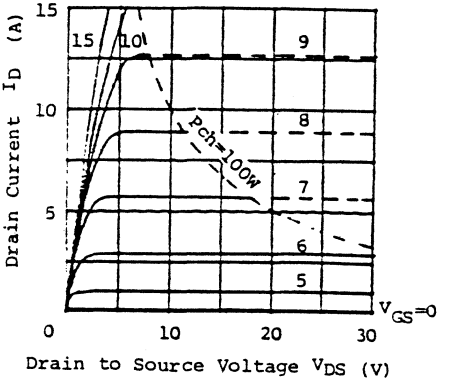
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	120	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=5A, V_{GS}=15V	-	1.0	1.5	V
Foward Transfer Admittance	Yfs	I_D=5A, V_{DS}=10V	1.5	2.0	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	1130	-	pF
Output Capacitance	Coss	"	-	650	-	pF
Reverse Transfer Capacitance	Crss	"	-	330	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	60	-	ns
Turn off Time	t_{off}	"	-	160	-	ns

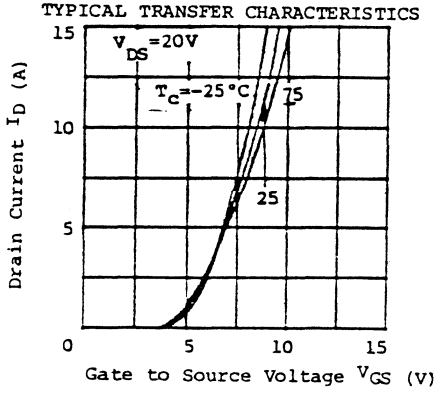
AREA OF SAFE OPERATION



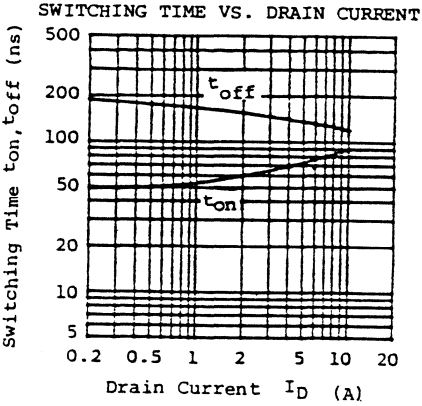
TYPICAL OUTPUT CHARACTERISTICS



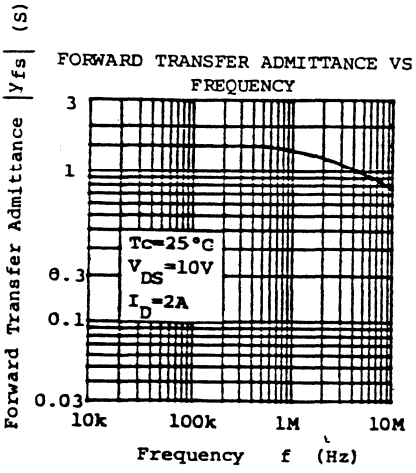
TYPICAL TRANSFER CHARACTERISTICS



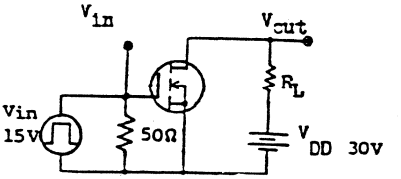
SWITCHING TIME VS. DRAIN CURRENT



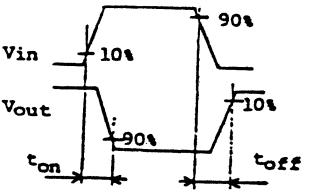
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



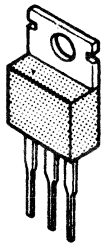
RESPONSE WAVE FORM



SILICON N CHANNEL MOS FET
HIGH SPPEED POWER SWICHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. Low On-Resistance.
2. High Speed Switching
3. High Cutoff Frequency.
4. No Secondary Breakdown.
5. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



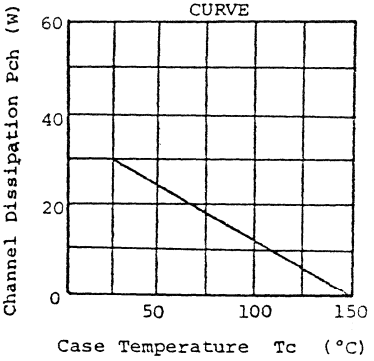
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating		Unit
		2SK310	2SK311	
rain to Source oltage	V_{DSS}	400	450	V
ate to Source Voltage	V_{GSS}	±20	±20	V
rain Current	I_D	3	3	A
rain Peak Current	$I_{D(peak)}$	6	6	A
hannel Dissipation	Pch*	30	30	W
hannel Temperature	Tch	150	150	°C
torage Temperature	Tstg	-55～150	-55～150	°C

*Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE

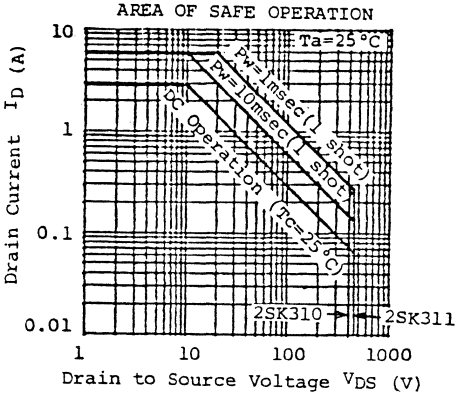


■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

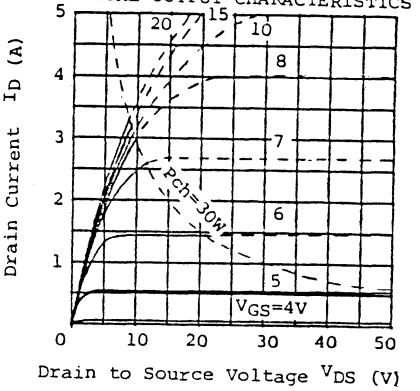
Item	Symbol	Test Condition	2SK310			2SK311			Unit
			min	typ	max	min	typ	max	
rain to Source reakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	-	-	450	-	-	V
ate to Source eak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	-	-	1	μA
rain Current	I_{DSS}	K310 V_{DS}=320V, V_{GS}=0	-	-	1	-	-	-	mA
		K311 V_{DS}=360V, V_{GS}=0	-	-	-	-	-	1	mA
ate to Source utoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	1.0	-	5.0	1.0	-	5.0	V
rain to Source aturation Voltage	$V_{DS(on)}$	V_{GS}=15V, I_D=2A*		5.0	8.0	-	5.0	8.0	V
orward Transfer dmittance	$\|y_{fs}\|$	V_{DS}=10V, I_D=2A*	0.6	1.0	-	0.6	1.0	-	S
Input Capacitance	Ciss	V_{GS}=0, V_{DS}=10V, f=1MHz	-	440	-	-	440	-	pF
Output Capacitance	Coss		-	95	-	-	95	-	pF
Reverce Transfer Capacitance	Crss		-	13	-	-	13	-	pF
Turn on Time	ton	V_{GS}=15V, I_D=2A, R_L=15Ω	-	25	-	-	25	-	ns
Turn off Time	toff		-	70	-	-	70	-	ns

*Pulse Test

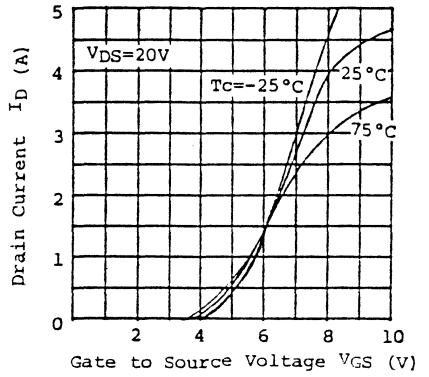
AREA OF SAFE OPERATION



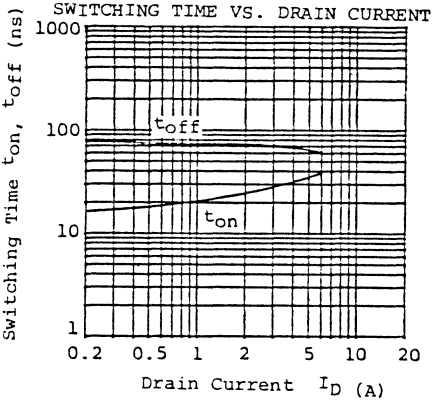
TYPICAL OUTPUT CHARACTERISTICS



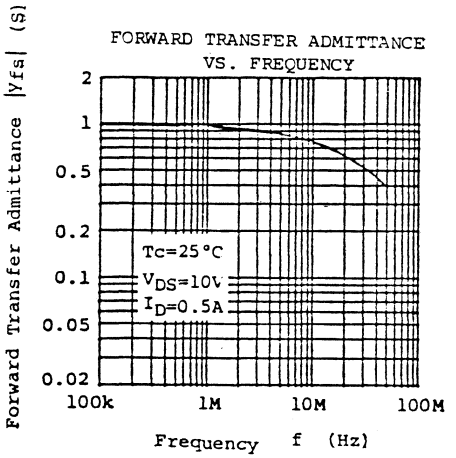
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



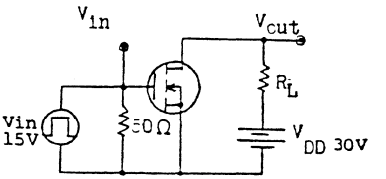
SWITCHING TIME VS. DRAIN CURRENT



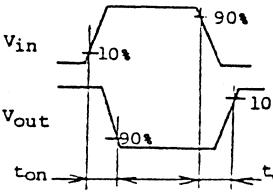
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



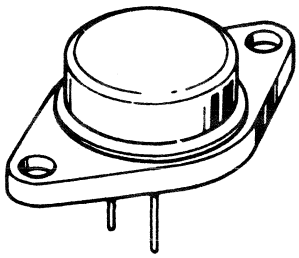
RESPONSE WAVE FORM



2SK312

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER
Features;

1. Low On-Resistance.
2. High Speed Switching.
3. High Cutoff Frequency.
4. No Secondary Breakdown.
5. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



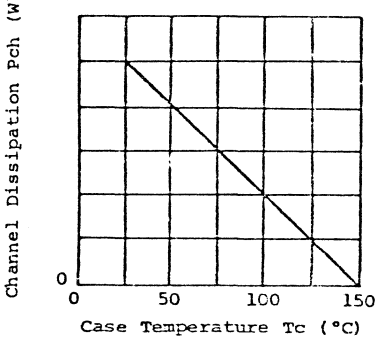
(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	400	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	12	A
Drain Peak Current	$I_{D(peak)}$	18	A
Channel Dissipation	Pch*	125	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

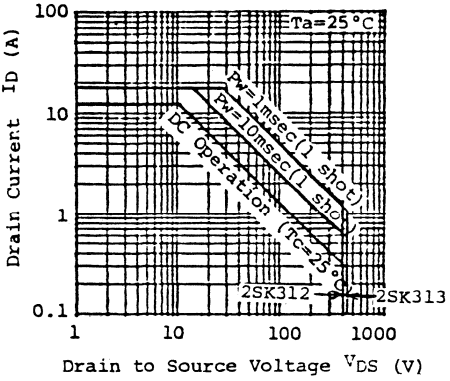
CHANNEL DISSIPATION CURVE



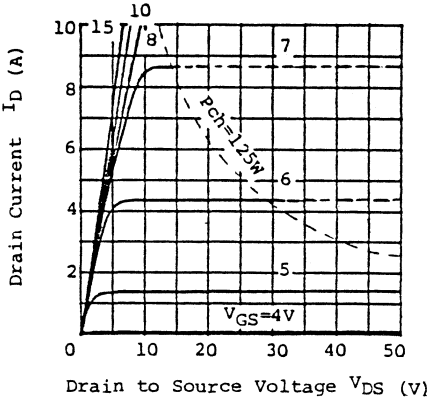
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=320V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=6A, V_{GS}=15V	-	4.0	5.4	V
Foward Transfer Admittance	$\|Yfs\|$	I_D=6A, V_{DS}=10V	1.5	2.5	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	1500	-	pF
Output Capacitance	Coss	"	-	330	-	pF
Reverse Transfer Capacitance	Crss	"	-	35	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	70	-	ns
Turn off Time	t_{off}	"	-	200	-	ns

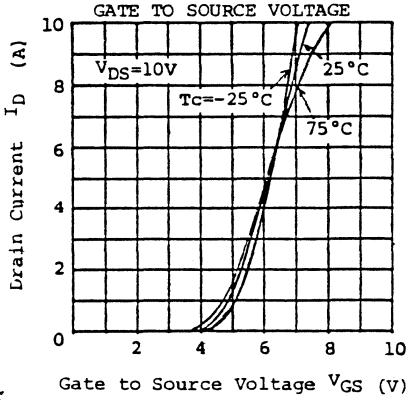
AREA OF SAFE OPERATION



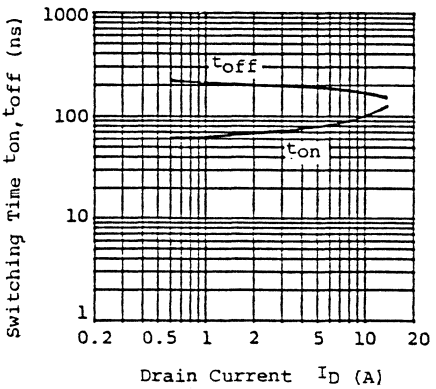
TYPICAL OUTPUT CHARACTERISTICS



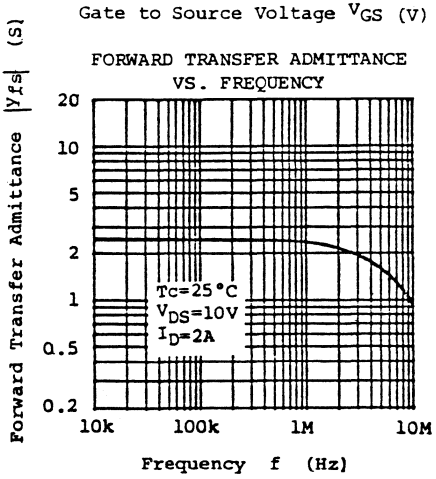
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



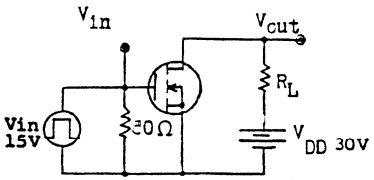
SWITCHING TIME VS. DRAIN CURRENT



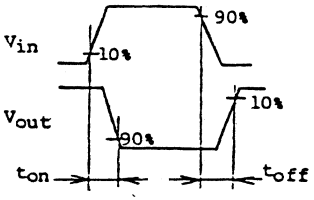
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM



SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
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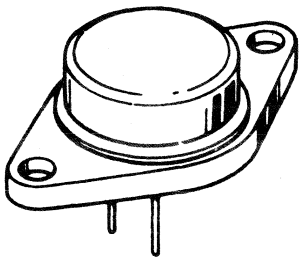
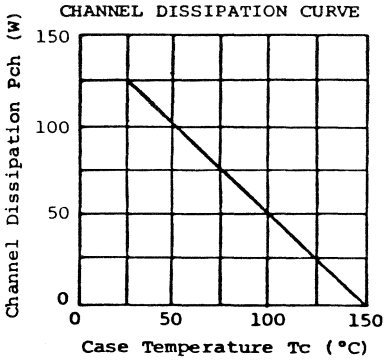


(JEDEC TO-3)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	450	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	12	A
Drain Peak Current	$I_{D(peak)}$	18	A
Channel Dissipation	Pch*	125	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

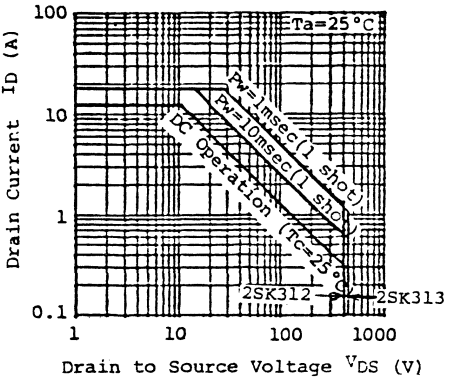
*Tc=25°C



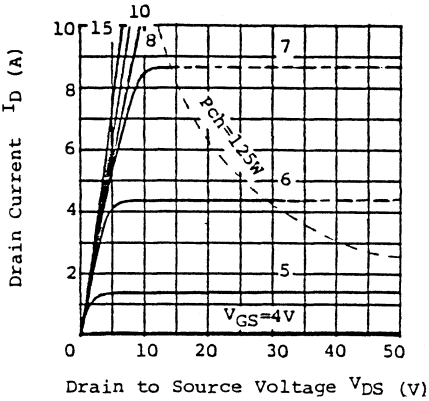
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=6A, V_{GS}=15V	-	4.0	5.4	V
Foward Transfer Admittance	$\|Yfs\|$	I_D=6A, V_{DS}=10V	1.5	2.5	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	1500	-	pF
Output Capacitance	Coss	"	-	330	-	pF
Reverse Transfer Capacitance	Crss	"	-	35	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	70	-	ns
Turn off Time	t_{off}	"	-	200	-	ns

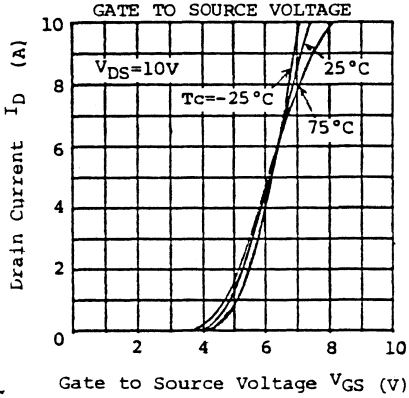
AREA OF SAFE OPERATION



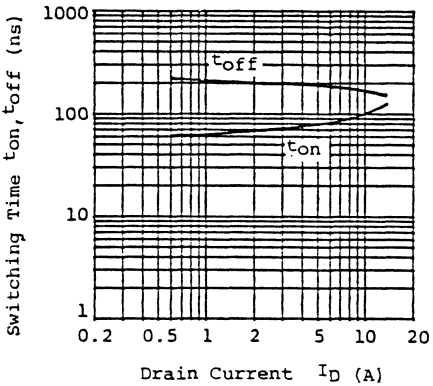
TYPICAL OUTPUT CHARACTERISTICS



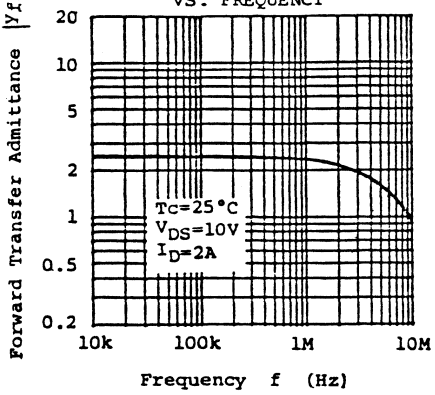
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



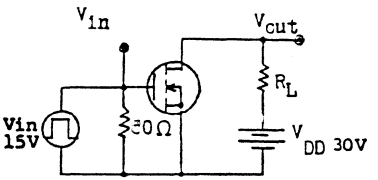
SWITCHING TIME VS. DRAIN CURRENT



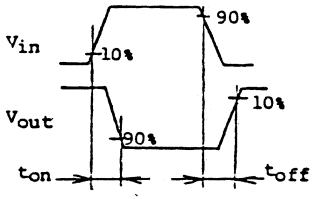
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT

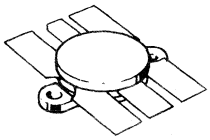


RESPONSE WAVE FORM



SILICON N-CHANNEL MOS FET
HF, VHF POWER AMPLIFIER

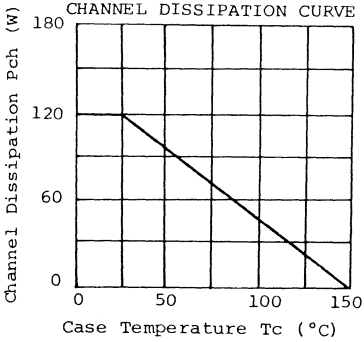
Features;
1. High Breakdown Voltage.
   You Can Decrease Handling Current.
2. Gate is Protected by Zenner Diodes.
3. No Secondary-Breakdown.
   Wide A.S.O.(Area of Safe Operation)
4. Infinite VSWR.
5. No Thermal Runaway.
6. Simple Bias Circuitry.



(RFPAK)

■ ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	180	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	8	A
Channel Dissipation	Pch*	120	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

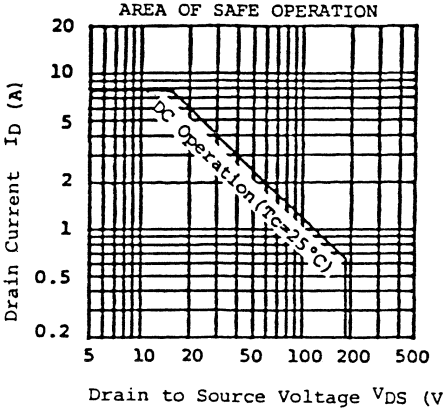


■ ELECTRICAL CHARACTERISTICS(Ta=25°C)

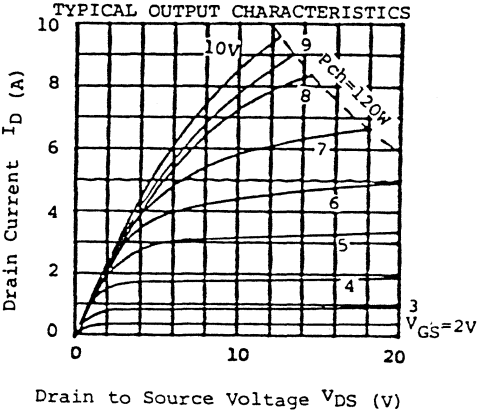
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Output	Po	V_{DS}=80V, I_{DQ}=0.1A	80	100	-	W
Drain Efficiency	η	Pin=8W, f=175MHz	-	(60)	-	%
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	180	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	0.5	-	3.0	V
Drain Current	I_{DSS}	V_{DS}=140V, V_{GS}=0	-	-	1.0	mA
Drain to Source Saturation Voltage	$V_{DS(on)}$	I_D=4A, V_{GS}=10V	-	3.8	5.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=20V	0.9	1.25	-	S
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=0, f=1MHz	-	600	-	pF
Output Capacitance	Coss	V_{GS}=-5V, V_{DS}=50V, f=1MHz	-	90	-	pF
Reverse Transfer Capacitance	Crss	V_{GD}=-50V, f=1MHz	-	0.5	-	pF

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

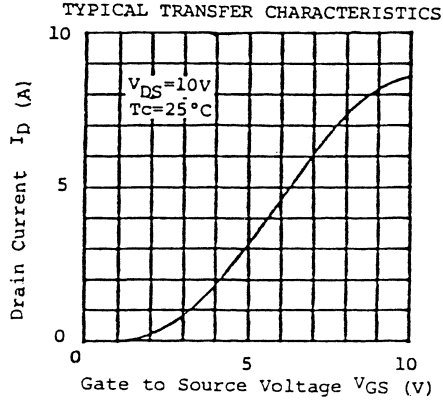
AREA OF SAFE OPERATION



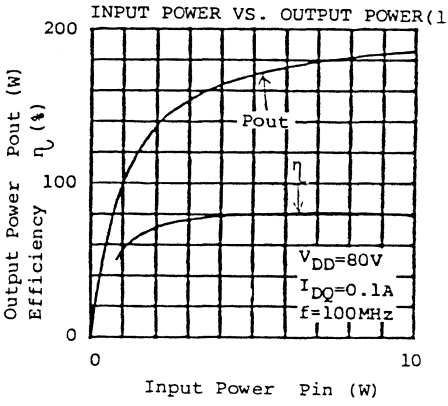
TYPICAL OUTPUT CHARACTERISTICS



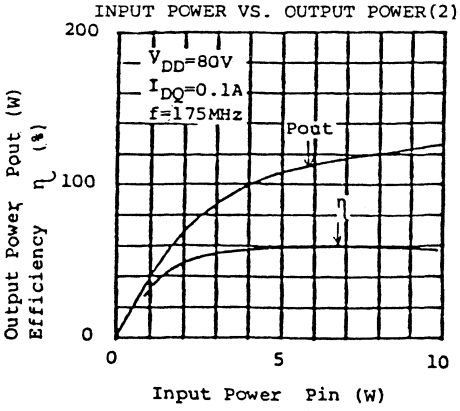
TYPICAL TRANSFER CHARACTERISTICS



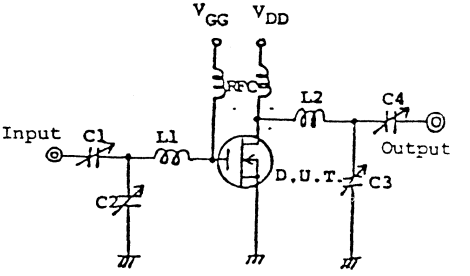
INPUT POWER VS. OUTPUT POWER(1)



INPUT POWER VS. OUTPUT POWER(2)



OUTPUT POWER TEST CIRCUIT



C1=22pF;C2=33pF;C3=10pF;C4=22pF

L1;L2 ID=6mm,d=1mm

f=100MHz L1=3T , L2=6T

f=175MHz L1=1T , L2=3T

Hitachi has developed the 2SK317, a power MOS FET (Metal-Oxide-Semiconductor, Field Effect Transistor) for high power output amplification for VHF band transmitters. The 2SK317 can be used for transmission in the VHF band up to 250MHz, allowing the highest power output, 180W at 100MHz, of all semiconductor devices.

Using the 2SK317 in parallel operation a compact amplifier in the class of several kilowatts can be built featuring high reliability, replacing the conventional vacuum tube type. The 2SK317 is expected to be highly useful in broadcasting systems of FM and TV stations and other communication systems.

Vacuum tubes have been predominant in the large-output transmitters in broadcast stations but have significant shortcomings: high running cost owing to the short service lives of vacuum tubes and the need for replacement every few years, large power consumption, and large size owing to the need for a cooling unit, large power source and other additional bulky equipment.

In the next stage of development, some solid-state transmitters using bipolar transistors were found to be unsatisfactory because the bipolar transistors tended to experience current concentration during operation, lacked thermal stability and were not suitable for delivering high power output in high voltage design applications and parallel operation.

On the other hand, the power MOS FET is not subject to current concentration compared to the bipolar transistor, and has a high destruction tolerance and good high-frequency characteristics in high voltage ranges, allowing parallel operation.

In addition to such basic features, Hitachi's new MOS FET 2SK317 is equipped with the following advantages:

(1) High drain-source breakdown voltage of 180V is three times as high as those of conventional transistors and can deliver an output three times greater.

(2) Because of high drain voltage, operating current is very low, allowing the delivery of high power output by connecting three times as many devices in parallel compared to bipolar transistors.

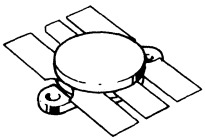
(3) Small reverse transfer capacitance allows simple circuit design.

(4) Since its gate is protected by zener diodes, static charge rupture strength is great.

In developing the 2SK317, the off-set gate structure having a field plate and the metal gate were adopted for the purposes of attaining a high breakdown voltage and desirable frequency characteristics.

2SK318

SILICON N-CHANNEL MOS FET
HF, VHF POWER AMPLIFIER

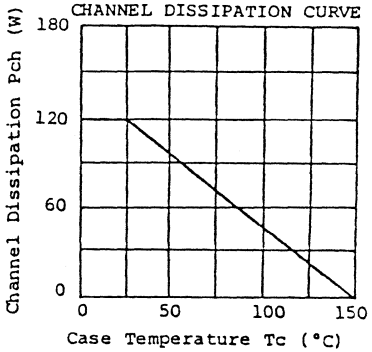


(RFPAK)

Features;
1. High Breakdown Voltage.
   You Can Decrease Handling Current.
2. Gate is Protected by Zenner Diodes.
3. No Secondary-Breakdown.
   Wide A.S.O.(Area of Safe Operation).
4. Infinite VSWR.
5. No Thermal Runaway.
6. Simple Bias Circuitry.

■ ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	180	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	4	A
Channel Dissipation	Pch*	70	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55~+150	°C

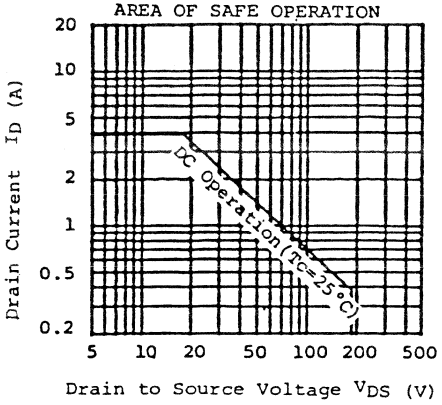


■ ELECTRICAL CHARACTERISTICS(Ta=25°C)

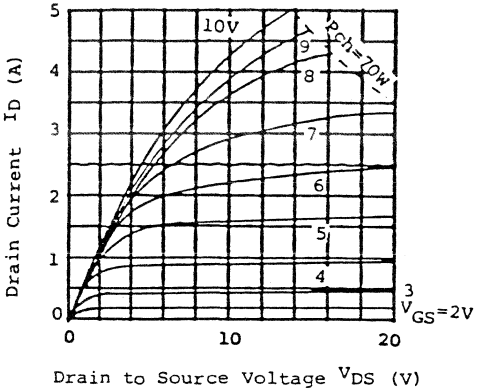
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Output	Po	V_{DS}=80V, I_{DQ}=0.1A	60	90	-	W
Drain Efficiency	η	Pin= 4W, f=100MHz	-	(80)	-	%
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	180	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G=±100μA, V_{DS}=0	±20	-	-	V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	0.5	-	3.0	V
Drain Current	I_{DSS}	V_{DS}=140V, V_{GS}=0	-	-	1.0	mA
Drain to Source Saturation Voltage	$V_{DS(on)}$	I_D=2A, V_{GS}=10V	-	3.8	6.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	I_D=1.5A, V_{DS}=20V	0.4	0.6	-	S
Input Capacitance	Ciss	V_{GS}=5V, V_{DS}=0, f=1MHz	-	300	-	pF
Output Capacitance	Coss	V_{GS}=-5V, V_{DS}=50V, f=1MHz	-	45	-	pF
Reverse Transfer Capacitance	Crss	V_{GD}=-50V, f=1MHz	-	0.3	-	pF

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

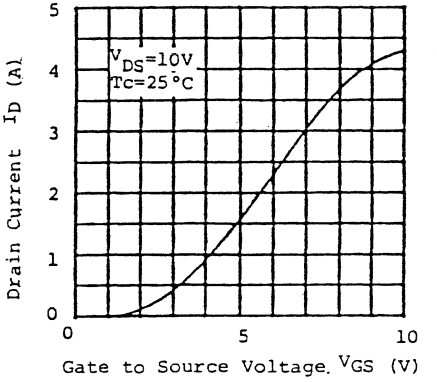
AREA OF SAFE OPERATION



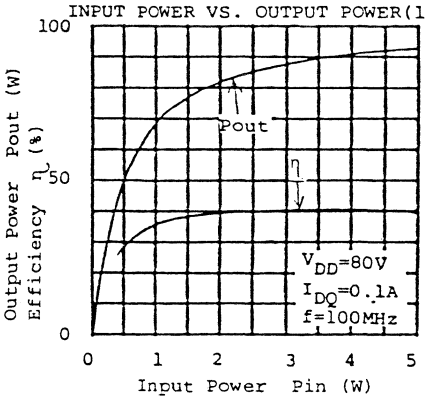
TYPICAL OUTPUT CHARACTERISTICS



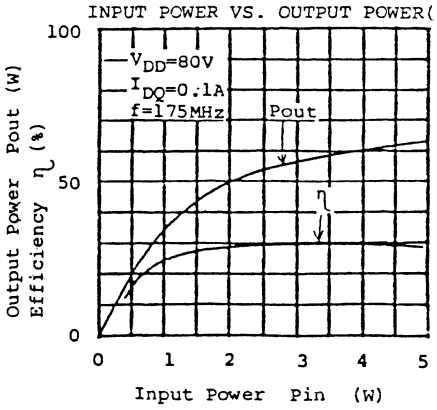
TYPICAL TRANSFER CHARACTERISTICS



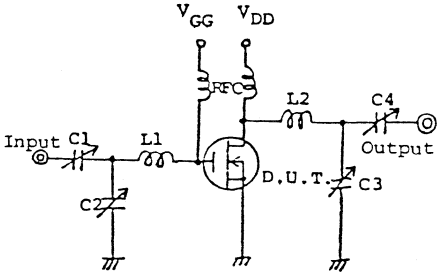
INPUT POWER VS. OUTPUT POWER(1)



INPUT POWER VS. OUTPUT POWER(2)



OUTPUT POWER TEST CIRCUIT



C1=22pF, C2=33pF, C3=25pF, C4=50pF

L1, L2 ID=6mm, d=1mm

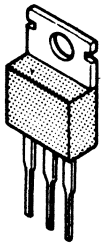
f=100MHz L1=3T, L2=5T

f=175MHz L1=1T, L2=3T

2SK319

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER
Features;

1. Low On-Resistance.
2. High Speed Switching.
3. High Cutoff Frequency.
4. No Secondary Breakdown.
5. Suitable for Switching Regulator, DC-DC Converter,
   RF Amplifiers, and Ultrasonic Power Oscillators.



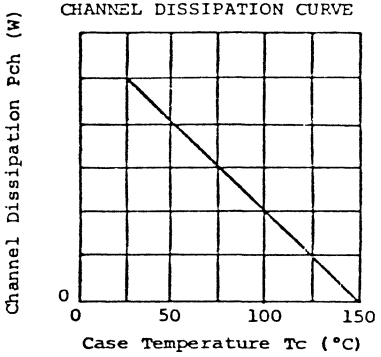
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	400	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(peak)}$	10	A
Channel Dissipation	Pch*	50	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

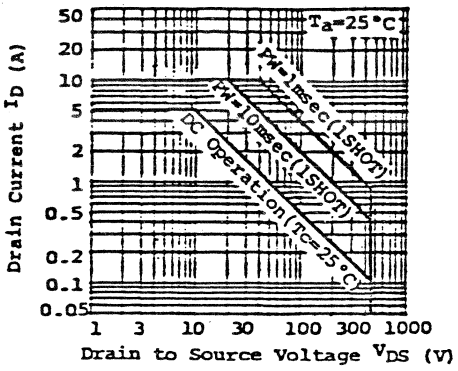
CHANNEL DISSIPATION CURVE



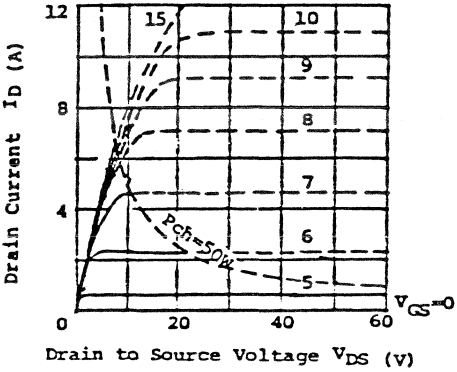
ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	400	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=320V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=3A, V_{GS}=15V	-	3.3	4.5	V
Foward Transfer Admittance	$\|Yfs\|$	I_D=3A, V_{DS}=10V	1.2	1.7	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	800	-	pF
Output Capacitance	Coss	"	-	180	-	pF
Reverse Transfer Capacitance	Crss	"	-	60	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	50	-	ns
Turn off Time	t_{off}	"	-	120	-	ns

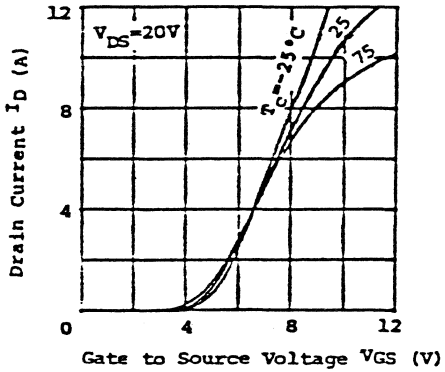
AREA OF SAFE OPERATION



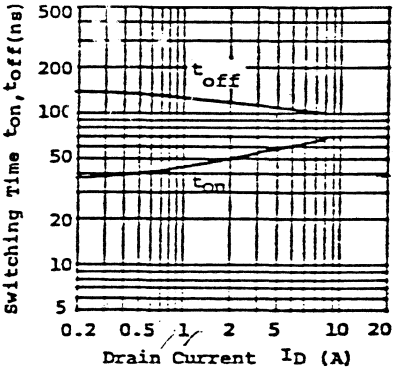
TYPICAL OUTPUT CHARACTERISTICS



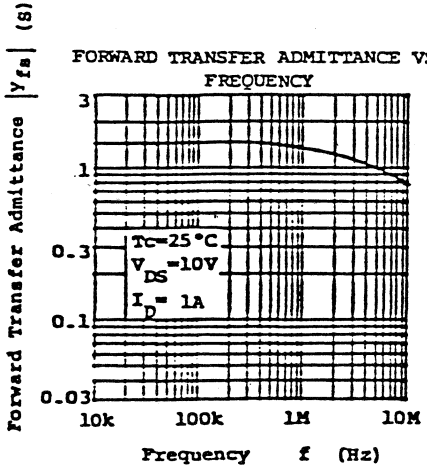
TYPICAL TRANSFER CHARACTERISTICS



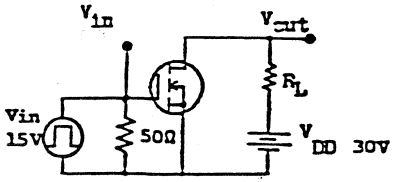
SWITCHING TIME VS. DRAIN CURRENT



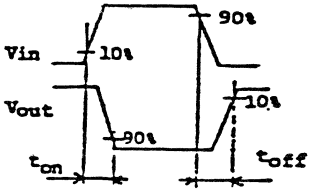
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



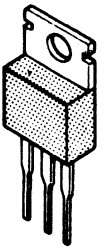
RESPONSE WAVE FORM



2SK320

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER
Features;

1. Low On-Resistance.
2. High Speed Switching.
3. High Cutoff Frequency.
4. No Secondary Breakdown.
5. Suitable for Switching Regulator, DC-DC Converter,
   RF Amplifiers, and Ultrasonic Power Oscillators.



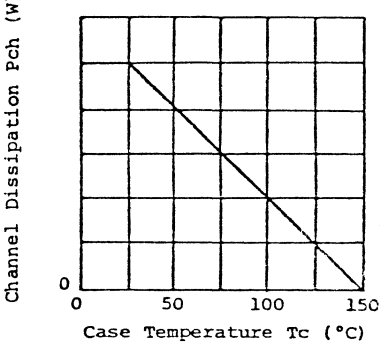
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	450	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(peak)}$	10	A
Channel Dissipation	Pch*	50	W
Channel Temperature	T_{stg}	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

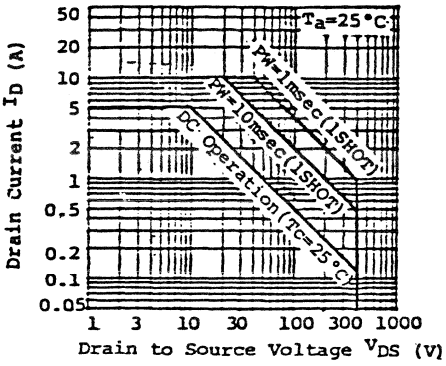
CHANNEL DISSIPATION CURVE



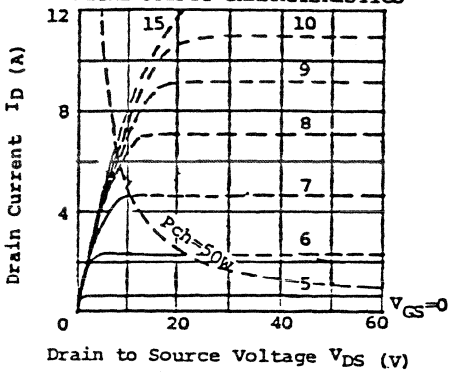
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	450	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=360V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	4.5	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=3A, V_{GS}=15V	-	3.3	4.5	V
Foward Transfer Admittance	$\|Yfs\|$	I_D=3A, V_{DS}=10V	1.2	1.7	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	800	-	pF
Output Capacitance	Coss	"	-	180	-	pF
Reverse Transfer Capacitance	Crss	"	-	60	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	50	-	ns
Turn off Time	t_{off}	"	-	120	-	ns

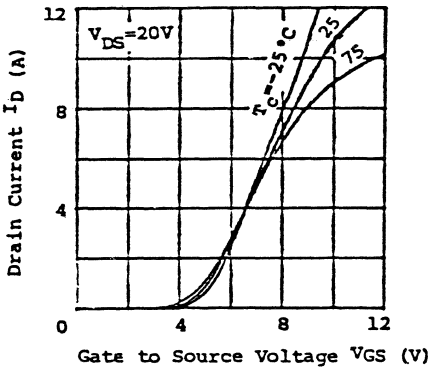
AREA OF SAFE OPERATION



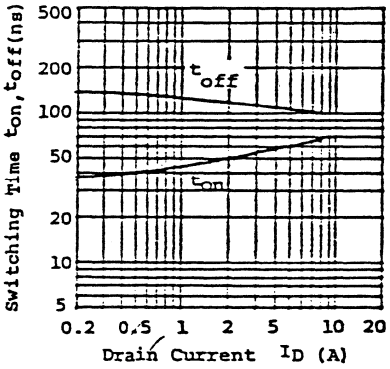
TYPICAL OUTPUT CHARACTERISTICS



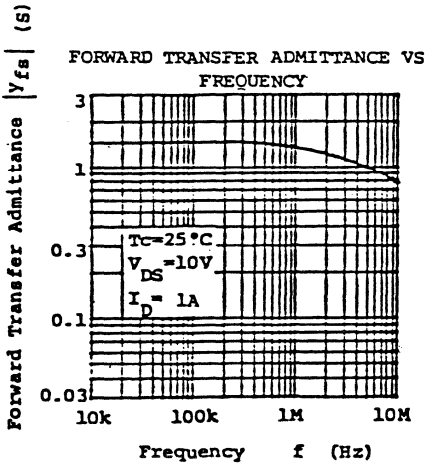
TYPICAL TRANSFER CHARACTERISTICS



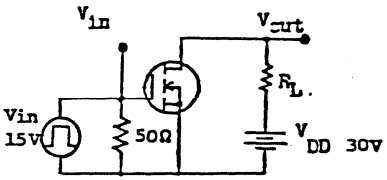
SWITCHING TIME VS. DRAIN CURRENT



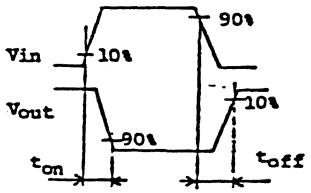
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM

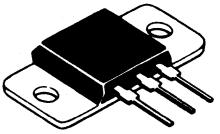


2SK343/344

SILICON N-CHANNEL ENHANCEMENT MOS FET
LOW FREQUENCY POWER AMPLIFIER,
HIGH SPEED AND POWER SWITCHING
Complementary pair with 2SJ99, 2SJ100

Feautres;

1. Low On-Resistance.
2. High Speed Switching.
3. No Secondary Breakdown.
4. Good Complementary Characteristics.



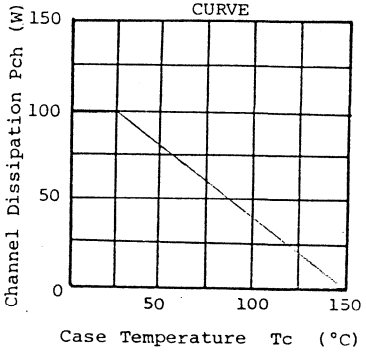
(HPAK)

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating		Unit
		2SK343	2SK344	
Drain to Source Voltage	V_{DSS}	140	160	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	8	8	A
Drain Peak Current	$I_{D(peak)}$	12	12	A
Channel Dissipation	Pch*	100	100	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	T_{stg}	-45～+150	-45～+150	°C

*Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE



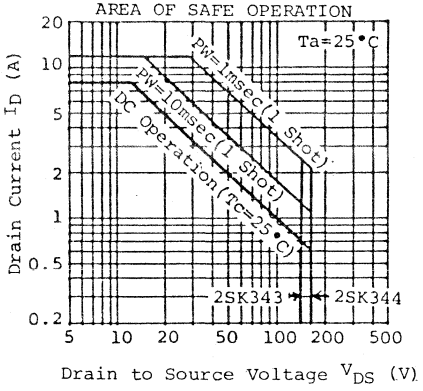
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	2SK343			2SK344			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	140	-	-	160	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	-	-	1	μA
Drain Current	I_{DSS}	K343 V_{DS}=120V, V_{GS}=0	-	-	1	-	-	-	mA
		K344 V_{DS}=140V, V_{GS}=0	-	-	-	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	2.0	-	5.0	2.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	V_{GS}=15V, I_D=4A*	-	1.6	2.0	-	1.6	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=10V, I_D=4A*	1.0	2.0	-	1.0	2.0	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	800	-	-	800	-	pF
Output Capacitance	Coss		-	330	-	-	330	-	pF
Reverce Transfer Capacitance	Crss		-	60	-	-	60	-	pF
Turn on Time	ton	V_{GS}=15V, I_D=2A	-	100	-	-	100	-	ns
Turn off Time	toff		-	90	-	-	90	-	ns

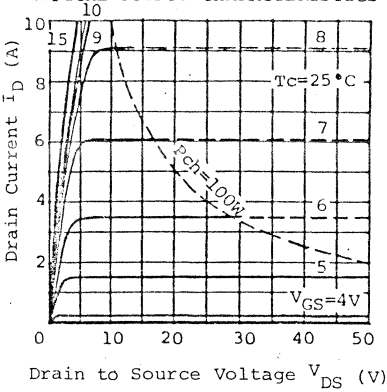
*Pulse Test

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

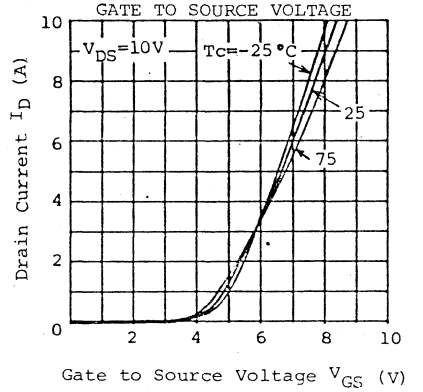
AREA OF SAFE OPERATION



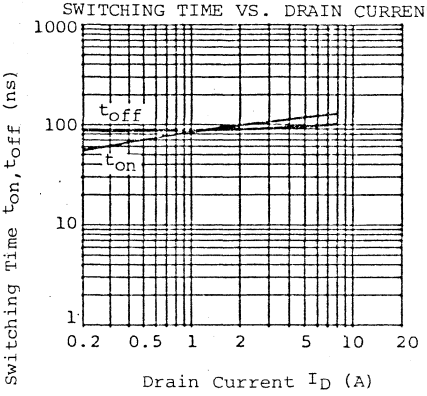
TYPICAL OUTPUT CHARACTERISTICS



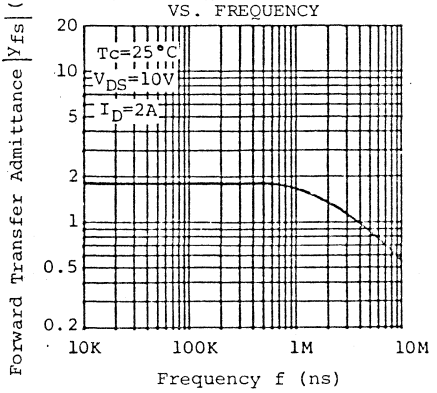
DRAIN CURRENT VS. GATE TO SOURCE VOLTAGE



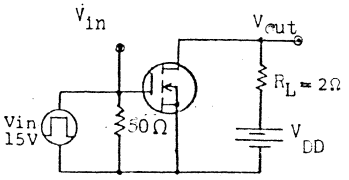
SWITCHING TIME VS. DRAIN CURRENT



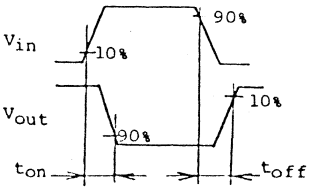
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVE FORM

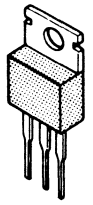


2SK345/346

SILICON N CHANNEL MOS FET
LOW FREQUENCY POWER AMPLIFIER.
HIGH SPEED POWER SWITCHING.
Complementary pair with 2SJ101,2SJ102.

Features;

1. Low On-Resistance.
2. High Speed Switching.
3. No Secondary Breakdown.
4. Good Complementary Characteristics.



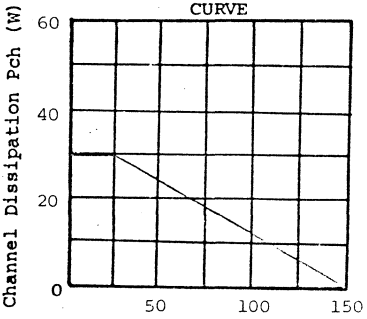
(JEDEC TO-220AB)

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Item	Symbol	Rating		Unit
		2SK345	2SK346	
Drain to Source Voltage	V_{DSS}	40	60	V
Gate to Source Voltage	V_{GSS}	±20	±20	V
Drain Current	I_D	5	5	A
Drain Peak Current	$I_{D(peak)}$	10	10	A
Channel Dissipation	Pch*	30	30	W
Channel Temperature	Tch	150	150	°C
Storage Temperature	T_{stg}	-45～+150	-45～+150	°C

*Value at Tc=25°C

MAXIMUM CHANNEL DISSIPATION CURVE



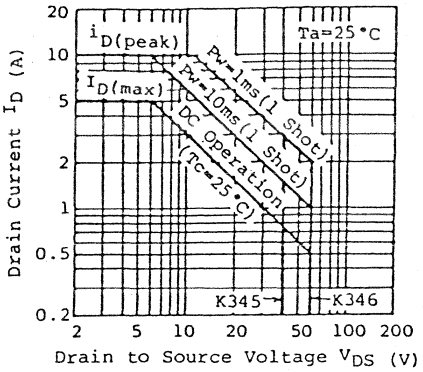
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	2SK345			2SK346			Unit
			min	typ	max	min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	40	-	-	60	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0	-	-	1	-	-	1	μA
Drain Current	I_{DSS} K345	V_{DS}=30V, V_{GS}=0	-	-	1	-	-	-	mA
	I_{DSS} K346	V_{DS}=50V, V_{GS}=0	-	-	-	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V , I_D=1mA	2.0	-	5.0	2.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(on)}$	V_{GS}=15V , I_D=3A*	-	0.9	1.2	-	0.9	1.2	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=10V , I_D=3A*	0.5	1.0	-	0.5	1.0	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	350	-	-	350	-	pF
Output Capacitance	Coss		-	300	-	-	300	-	pF
Reverce Transfer Capacitance	Crss		-	80	-	-	80	-	pF
Turn on Time	ton	V_{GS}=15V , I_D=2A	-	30	-	-	30	-	ns
Turn off Time	toff		-	40	-	-	40	-	ns

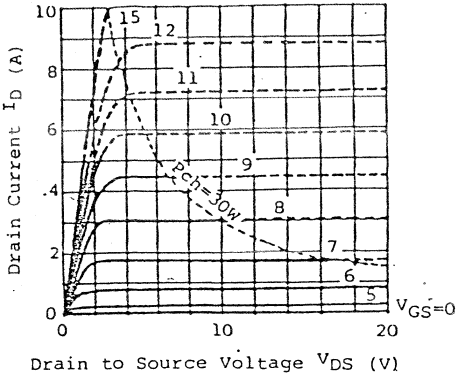
*Pulse Test

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

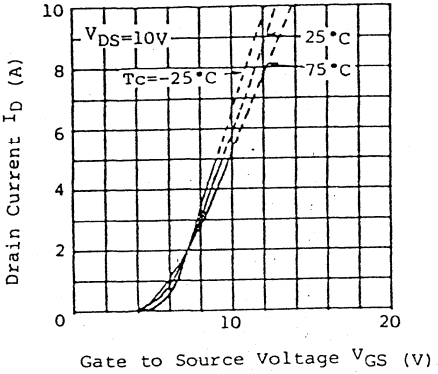
AREA OF SAFE OPERATION



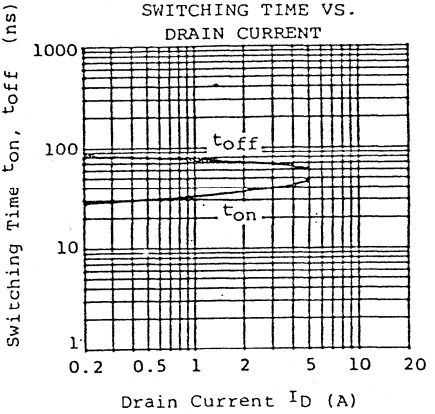
TYPICAL OUTPUT CHARACTERISTICS



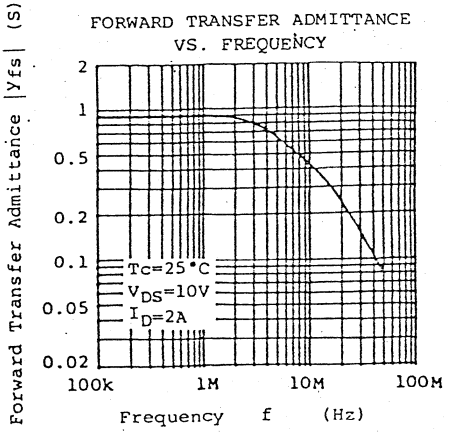
TYPICAL TRANSFER CHARACTERISTICS



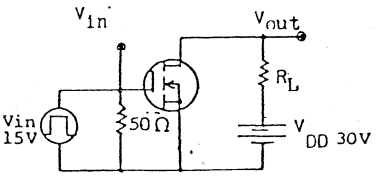
SWITCHING TIME VS. DRAIN CURRENT



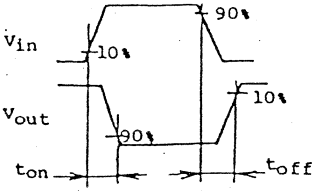
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TESTING CIRCUIT



RESPONSE WAVE FORM

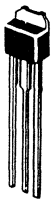


2SK347

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. Small Package.
2. High Speed Switching.
3. High Cutoff Frequency.
4. No Secondary Breakdown.
5. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.

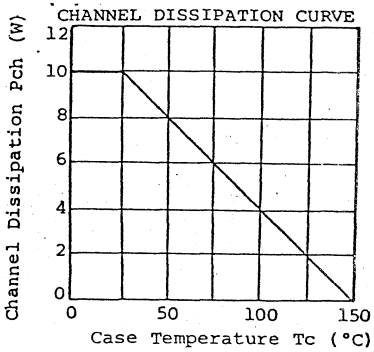


(DPAK)

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	400	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	1	A
Drain Peak Current	$I_{D(peak)}$	2	A
Channel Dissipation	Pch*	10	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-45~+150	°C

*Tc=25°C

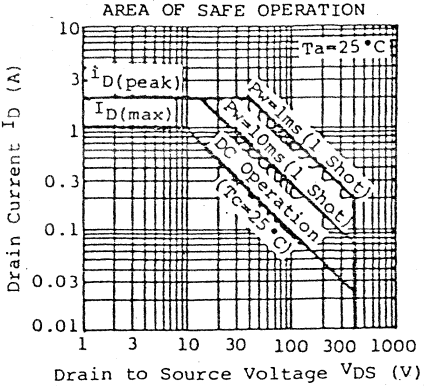


ELECTRICAL CHARACTERISTICS (Ta=25°C)

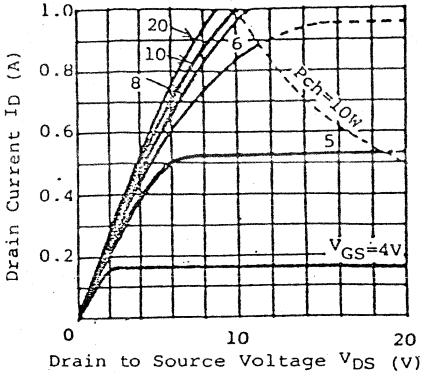
Item	symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	400	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0	-	-	±1	μA
Drain Current	I_{DSS}	V_{DS}=320V , V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=0.5A , V_{GS}=15V	-	4.5	6.0	V
Foward Transfer Admittance	$\|Yfs\|$	I_D=0.5A , V_{DS}=10V	100	200	-	mS
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	125	-	pF
Output Capacitance	Coss	"	-	40	-	pF
Reverse Transfer Capacitance	Crss	"	-	6	-	pF
Turn on Time	t_{on}	I_D=0.5A, V_{GS}=15V, R_L=60Ω	-	20	-	ns
Turn off Time	t_{off}	"	-	40	-	ns

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

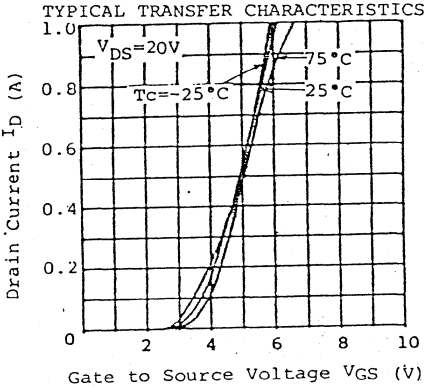
AREA OF SAFE OPERATION



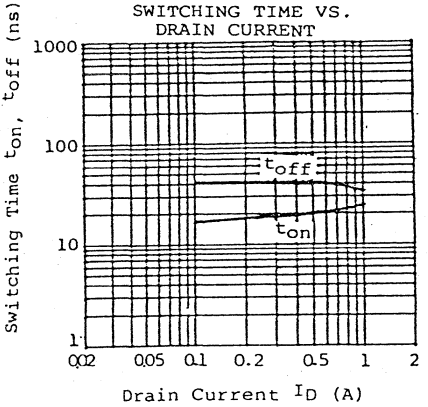
TYPICAL OUTPUT CHARACTERISTICS



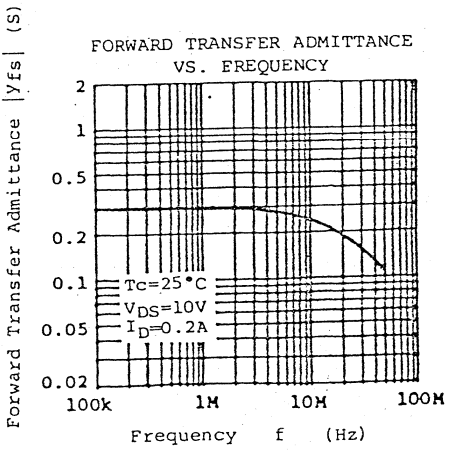
TYPICAL TRANSFER CHARACTERISTICS



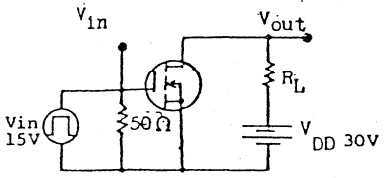
SWITCHING TIME VS. DRAIN CURRENT



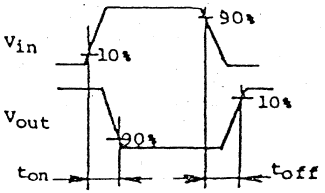
FORWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TESTING CIRCUIT



RESPONSE WAVE FORM

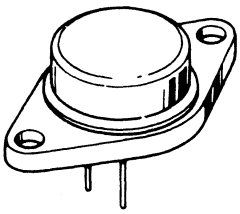


2SK351

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

Features;

1. High Breakdown Voltage.
2. High Speed Switching.
3. High Cutoff Frequency.
4. No Secondary Breakdown.
5. Suitable for Switching Regulator, DC-DC Converter, RF Amplifiers, and Ultrasonic Power Oscillators.



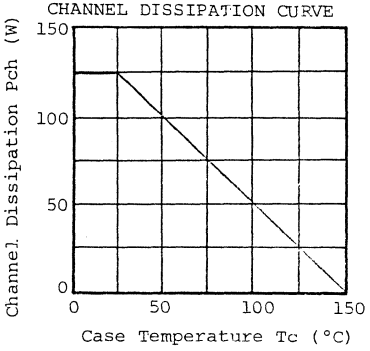
(JEDEC TO-3)

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	800	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	5	A
Drain Peak Current	$I_{D(peak)}$	10	A
Channel Dissipation	Pch*	125	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

*Tc=25°C

CHANNEL DISSIPATION CURVE



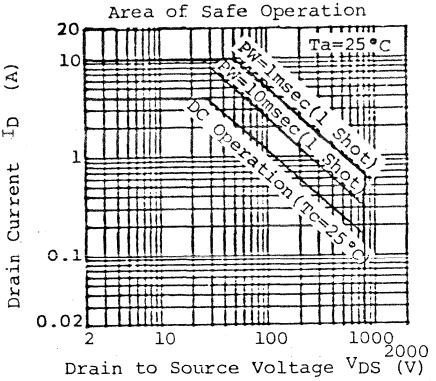
ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0	800	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0	-	-	1	uA
Drain Current	I_{DSS}	V_{DS}=640V, V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA, V_{DS}=10V	1.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=3A, V_{GS}=15V *	-	5.0	9.0	V
Foward Transfer Admittance	$\|y_{fs}\|$	I_D=3A, V_{DS}=10V *	1.0	2.0	-	S
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	1900	-	pF
Output Capacitance	Coss	"	-	320	-	pF
Reverse Transfer Capacitance	Crss	"	-	40	-	pF
Turn on Time	t_{on}	I_D=2A, V_{GS}=15V, R_L=15Ω	-	100	-	ns
Turn off Time	t_{off}	"	-	300	-	ns
Fall Time	t_f	"	-	80	-	ns

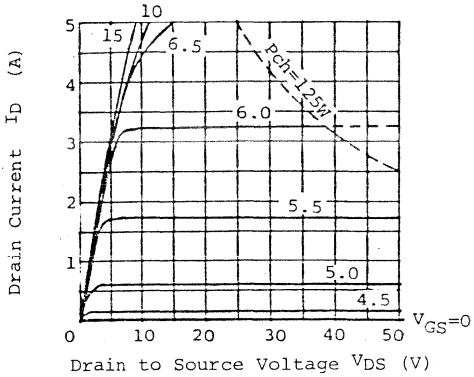
Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications

*Pulse Test

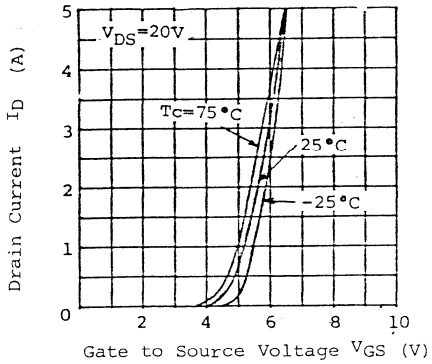
Area of Safe Operation



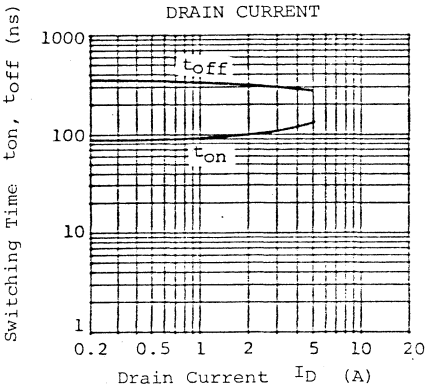
TYPICAL OUTPUT CHARACTERISTICS



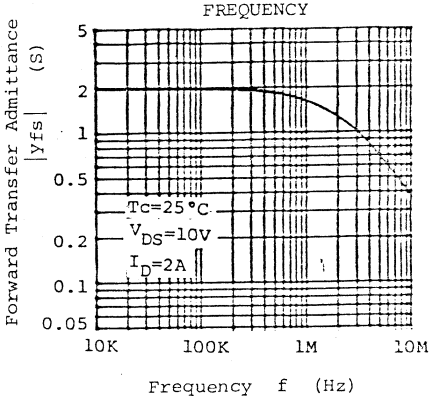
TYPICAL TRANSFER CHARACTERISTICS



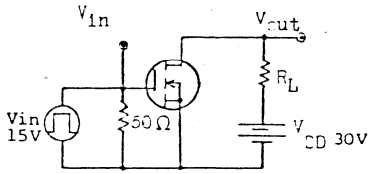
SWITCHING TIME VS. DRAIN CURRENT



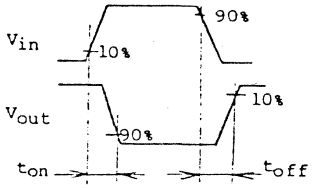
FOWARD TRANSFER ADMITTANCE VS. FREQUENCY



SWITCHING TIME TEST CIRCUIT



RESPONSE WAVEFORM



2SK352

SILICON N-CHANNEL MOS FET
HIGH SPEED POWER SWITCHING,
HIGH FREQUENCY POWER AMPLIFIER

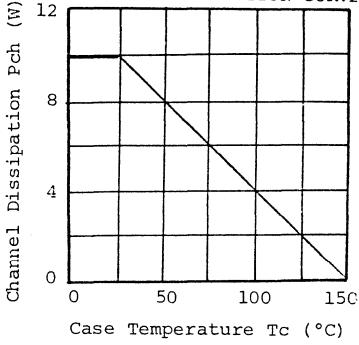
(JEDEC TO-126 mod)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	250	V
Gate to Soure Voltage	V_{GSS}	±15	V
Drain Current	I_D	0.3	A
Drain peak Current	$I_{D(peak)}$	0.5	A
Channel Dissipation	Pch*	10	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55~+150	°C

*Tc=25°C

CHANNEL DISSIPATION CURVE



■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA , V_{GS}=0	250	-	-	V
Gate to Source Leak Current	I_{GSS}	V_{GS}=±15V , V_{DS}=0	-	-	1	μA
Drain Current	I_{DSS}	V_{DS}=200V , V_{GS}=0	-	-	1	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D=1mA , V_{DS}=10V	1.0	-	5.0	V
Drain to Source Saturation Voltage	$V_{DS(ON)}$	I_D=0.1A , V_{GS}=15V	-	3.0	-	V
Foward Transfer Admittance	$\|Y_{fs}\|$	I_D=0.15A , V_{DS}=10V	-	80	-	mS
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0, f=1MHz	-	20	-	pF
Output Capacitance	Coss	"	-	10	-	pF
Reverse Transfer Capacitance	Crss	"	-	2.5	-	pF

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Application Information

3.1 Output Characteristics

Figs. 3-1 and 3-2 show the output characteristics of the N-channel MOS FET 2SK135. Whereas in a small signal MOS FET the forward transconductance y_{fs} is 10 ~ 20 mS (milli-siemens) at best, in a power MOS FET it is 1.0 S. Also, as obvious from Figs. 3-1 and 3-2, 2SK135 has pentode characteristics and an excellent linearity of y_{fs} in relation to I_D.

P channel MOS FETs also have similar characteristics. P channel and N channel types have complementary characteristics.

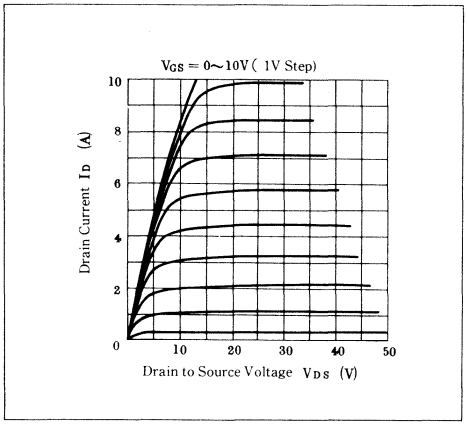


Fig.3-1 Typical Output Characteristics (1)

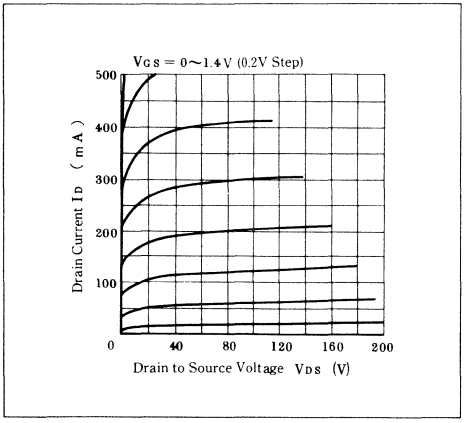


Fig.3-2 Typical Output Characteristics (2)

3.2 Frequency Response Characteristics

Fig. 3-3 shows the frequency response characteristics of a power MOS FET in the source common state. The cut-off frequency of an N channel device is about 3 MHz. The frequency response is dependent on the gate resistance and input capacitance shown in Fig. 2-2.

In the output stage of an audio amplifier, a source follower is used. The frequency response of the source follower is 10 times greater than in the case of source common because, as shown in Fig. 3-4, input capacitance is reduced by the mirror effect. The frequency response of a power MOS FET is more than one order better than that of a bipolar transistor.

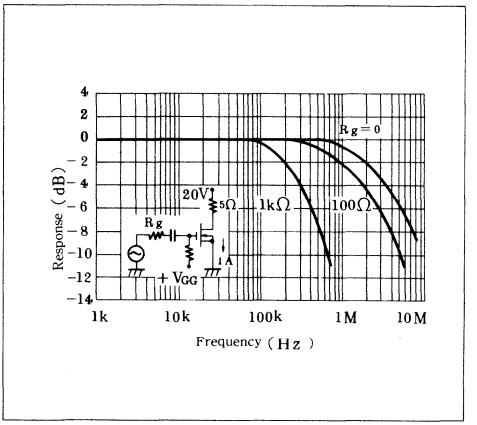


Fig.3-3 Frequency Response Characteristics of |Yfs| (Source Common)

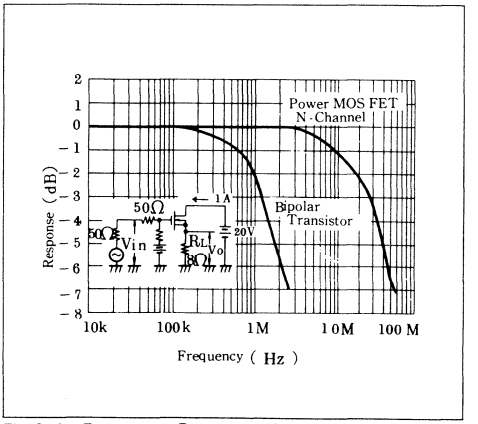


Fig.3-4 Frequency Response Characteristics of Source Follower

3.3 Switching Characteristics

A power MOS FET has no minority carrier storage and can switch a 2 A current at speed of 10 ~ 30 ns. This switching speed is 50 ~ 100 times as high as that of a bipolar transistor and represents a great advantage when a power MOS FET is applied to various high-speed large-power switching circuits, such as described later in this application note.

Fig. 3-5 shows current waveforms where a power MOS FET is applied to a class-B amplifier stage of an audio amplifier. The waveform is ideal for a power MOS FET which, unlike a bipolar transistor, has no storage time.

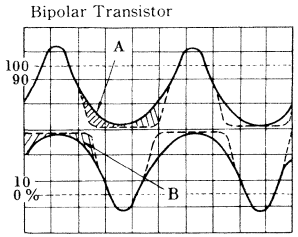


Fig.3-5 Current Waveform of Class-B Amplifier Stage

3.4 Area of Safe Operation (A.S.O.)

Since a power amplifier device is operated at high voltage and high current levels, it must be designed to withstand electrical destruction. A power MOS FET basically takes full advantage of its excellent thermal stability, so that a much wider area of safe operation can be guaranteed for it than for a bipolar transistor.

Fig. 3-6 shows the areas of safe operation for DC operation and pulse operation. Since a power MOS FET is free of secondary breakdown in the high voltage region, the guaranteed area of safe operation is equal to the range of thermal limitation.

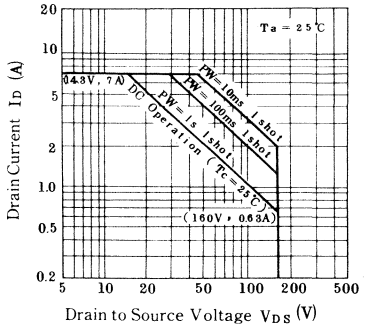


Fig.3-6 Area of Safe Operation (2SK135/2SJ50)

3.5 Temperature Characteristics

Fig. 3-7 shows the transfer characteristics of power MOS FETs. In the high current area, the temperature coefficient is negative and current concentration does not occur, so that a wide area of safe operation is provided and destruction by thermal runaway is largely prevented. Since the transfer characteristics of power MOS FETs are of the enhancement type, as in the case of bipolar transistors, power MOS FETs do not require a complex biasing circuit as depletion type FETs do.

In power MOS FETs, the temperature coefficient of drain current becomes zero around I_D = 100 mA.

By taking advantage of these temperature characteristics, the power MOS FET circuit can dispense with an idling current compensation circuit and feedback resistance for current stabilization, which are required in the bipolar transistor circuit as shown in Fig. 3-8. Hence, a simple circuitry as shown in Fig. 3-9 is obtained.

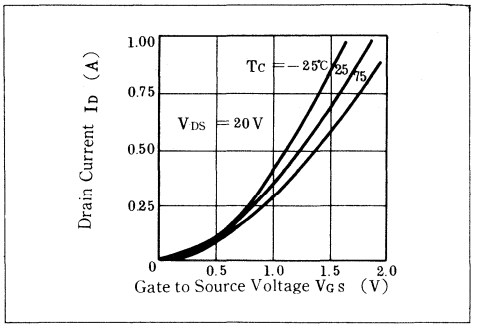


Fig.3-7 Typical Transfer Characteristics

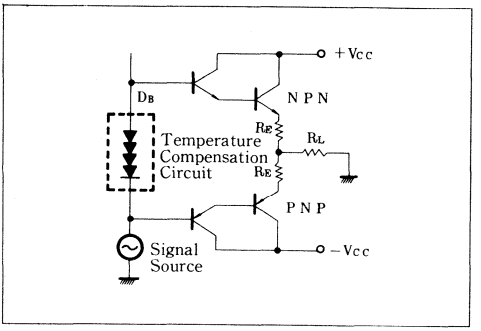


Fig.3-8 Audio Output Circuit using of Bipolar Transistor

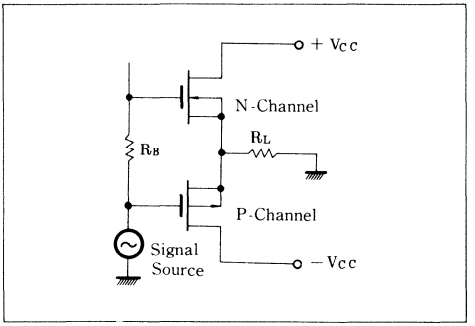


Fig.3-9 Audio Output Circuit using of Power MOS FET

4.1 Design of High Power Application (Parallel Operation)

As stated in section 3.5, the negative temperature coefficient of drain current and the high input impedance of power MOS FETs enable parallel operation to be performed with an extremely simple circuit.

In the parallel operation of bipolar power transistors, scattering of V_{BE} and h_{FE} characteristics causes an unbalance in collector current and, as a result, large current transistors generate high heat, which in turn further increases current flow; this may lead to thermal runaway. In a power MOS FET there is no possibility of thermal runaway because the drain current has a negative thermal coefficient.

Fig. 4-1 shows a triple connection circuit. Forward transfer admittance is three times as large as when a single device is used. In Figs. 4-2 and 4-3, this is expressed in waveform on a curve tracer. A current of about 20 A can be controlled by several volts of gate voltage.

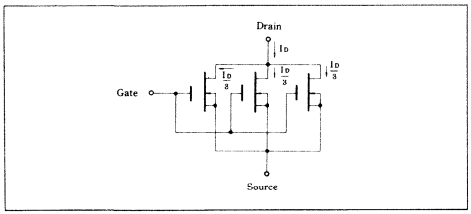


Fig.4-1 Triple Connection Circuit (Example of the N-Channel Device)

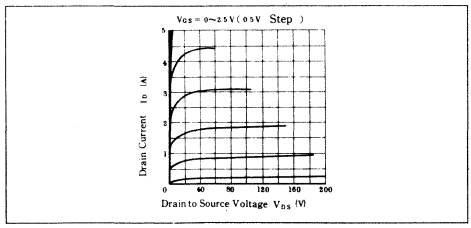


Fig.4-2 Output Characteristics in Triple Connection Circuit(1)

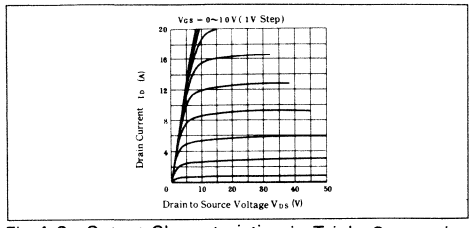


Fig.4-3 Output Characteristics in Triple Connection Circuit(2)

4.2 Design of High Breakdown Voltage Application (Series Operation)

(1) Totem pole connection

Fig. 4-4 shows a basic "totem pole" circuit, in which power MOS FETs are connected in series. This circuit has been used extensively as a saturated logic circuit, the basic circuitry for TTL IC. Operation of this circuit will be explained.

When no bias is applied to Q_1, Q_1 is cut off because power MOS FETs have enhancement type transfer characteristics; thus the following relationships hold;

$$V_{G1} = 0, \quad I_D = 0$$

$$V_{G2} = {}^1\!/_2 V_{DD} \left(\because V_{G2} = V_{DD} \cdot \frac{Rg}{Rg + Rg} \right)$$

$$V_O = V_{G2} - V_{GS2}$$

$$= {}^1\!/_2 V_{DD} - V_{th2}$$

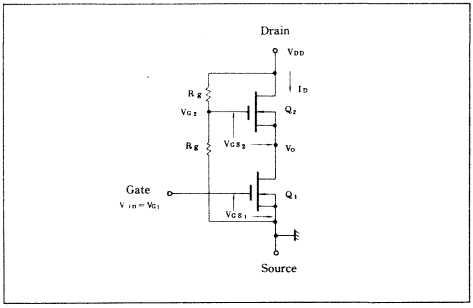


Fig.4-4 Basic Totem Pole Circuit

where V_{th2} is the threshold voltage of Q_2. Generally, $V_{th2} \ll V_{DD}$. Therefore $V_O \simeq {}^1\!/_2 V_{DD}$.
And the voltage applied to Q_1 and Q_2 will be about ½V_{DD}

Next, let us consider a transient state. When the gate bias of Q_1 is increased gradually from zero, Q_1 will become conductive and so will Q_2 at the same time. If load resistance Z_L is inserted between V_{DD} and drain of Q_2, drain voltage will be $V_D = V_{DD} - Z_L \cdot I_D$ and V_O ($= {}^1\!/_2 V_D - V_{GS2}$) will gradually decrease.

If V_{DD} has a much larger value than V_{GS2} and Q_2 is driven up to the saturation region, then the characteristics of an equivalent MOS FET would be dependent on Q_1.

Generally, when devices are operated in series, voltage unbalance due to switching time difference presents a problem. This problem is overcome in power MOS FETs because switching time can be made as short as several tens of nanoseconds.

Figs. 4-5 and 4-6 show breakdown and output characteristics where a single device is used. When this device is used in the circuit shown in Fig. 4-4, the breakdown and output characteristics would be as shown is Figs. 4-7 and

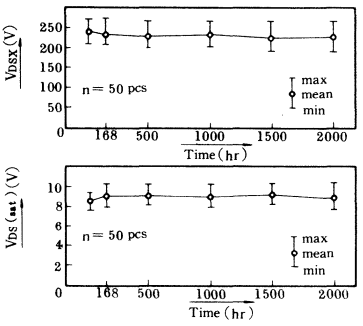
Table 3-3 Changes of Major Parameters

Type No.	2 S K 1 3 5
Test item	High temperature reverse bias test
Test condition	Ta = 150℃ V_{DSX} = 160 V, V_{GS} = − 10 V
Failure criteria	V_{DSX} = higher then 128 V $V_{DS(sat)}$ = lower then 14.4 V $\triangle V_{DS(sat)}$ = within ± 30 %
Failure mode	Surface degradation

Description

1. There is almost no breakdown voltage change after 2,000 hours.
2. Change of V_{DS}(sat) increases a little at the initial period, but the changes is completely saturated after 2,000 hours.
3. There is almost no degradation of V_{GSS} |yfs| and other parametes.

Changes of breakdown voltage and saturation voltage



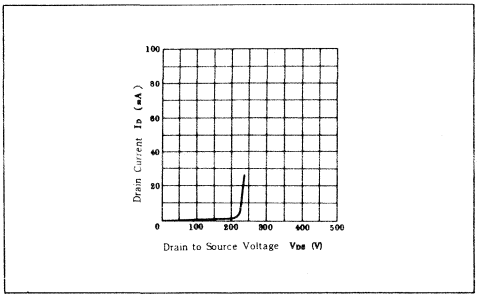


Fig.4-5 Breakdown Characteristics (Single Device)

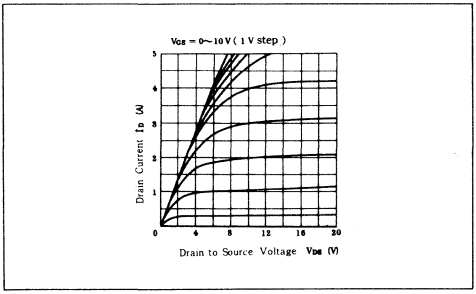


Fig.4-6 Output Characteristics (Single Device)

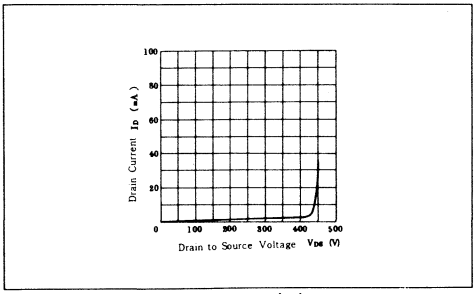


Fig.4-7 Breakdown Characteristics

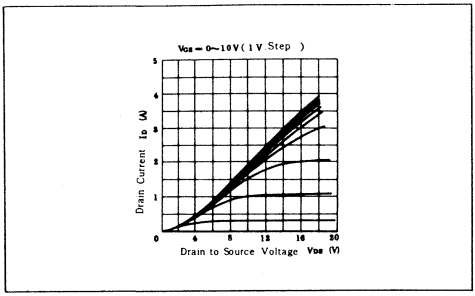


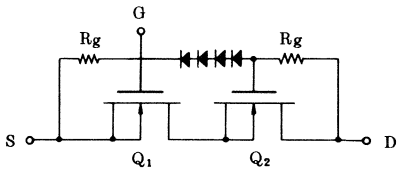
Fig.4-8 Output Characteristics

4-8. Breakdown voltage in Fig. 4-7 is twice as high as in Fig. 4-5. The disadvantage is that on-resistance is also doubled, as is obvious from Figs. 4-8 and 4-6. A method of improving on-resistance is described in the following section.

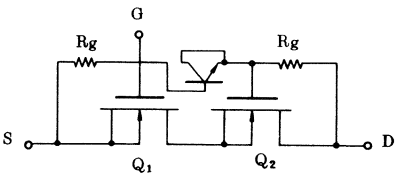
(2) How to reduce on-resistance in basic circuit

On-resistance (or saturation voltage) can be reduced by performing level shift of the Q_2 gate potential in the positive direction. This can be accomplished, for instance, by the methods shown in Fig. 4-9. Fig. 4-10 shows the output characteristics for a case where the gate is level-shifted to the positive side. (14 V is the maximum allowable gate-to-source voltage.)

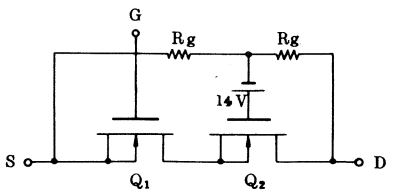
In the circuit shown in Fig. 4-9, as in the basic circuit, the equivalent drain to source breakdown voltage is twice as high as when a single device is used.



(A) Level Shift by Using of Diode



(B) Level Shift by Using of Breakdown Voltage in External Transistor



(C) Level Shift by Using of External Power Supply

Fig.4-9 How to Reduce ON—Resistance

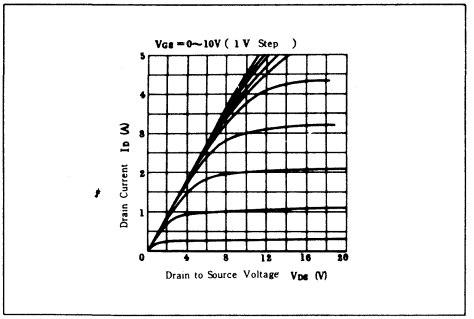


Fig.4-10 Output Characteristics ((C)Circuit)

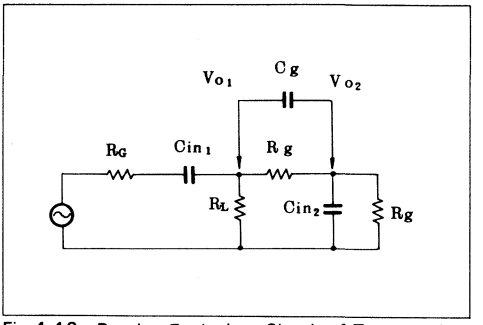


Fig.4-12 Passive Equivalent Circuit of Totem pole

(3) Improvement of high frequency characteristics in totem pole connection

When the circuit shown in Fig. 4-4 is modified for a source follower, because of the different operation of Q_1 and Q_2, a phase differential occurs under the influence of the power MOS FET input capacitance (about 500 pF for 2SK134, 600 pF for 25J49, f=1 MHz). As a result, characteristics worsen, as high frequency gain drops and phase shift increases.

This is expressed in Fig. 4-11. The equivalent circuit with passive devices alone is represented in Fig. 4-12.

It has been verified experimentally that the phase differential of V_{O1} and V_{O2} can be eliminated and driving in the same phase can be achieved by equalizing C_g with C_{in2} and that phase shift as 100 kHz can be limited within −90 degrees.

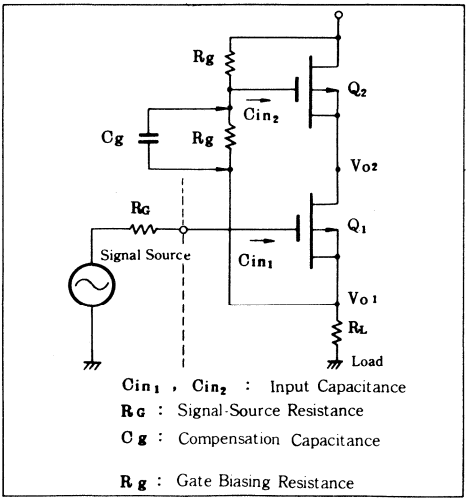


Fig.4-11 Improved Totem Pole Circuit

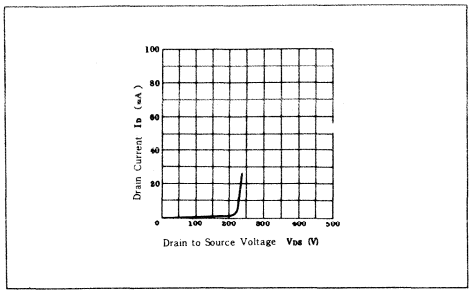


Fig.4-5 Breakdown Characteristics (Single Device)

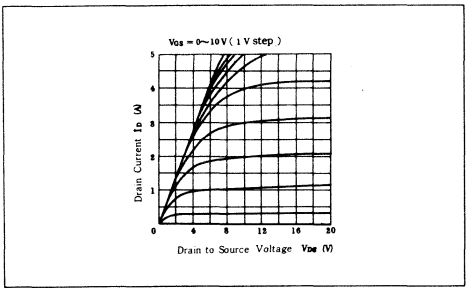


Fig.4-6 Output Characteristics (Single Device)

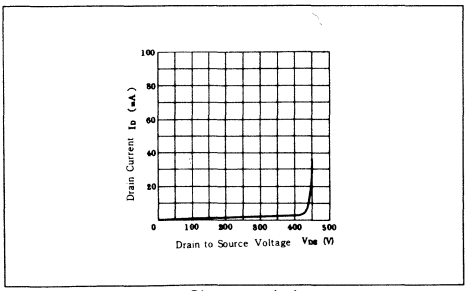


Fig.4-7 Breakdown Characteristics

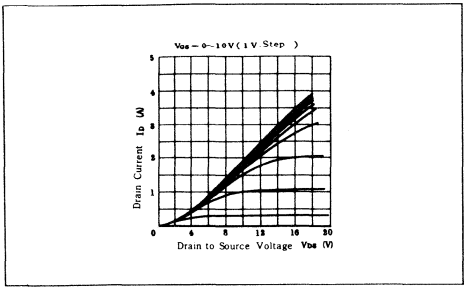


Fig.4-8 Output Characteristics

4-8. Breakdown voltage in Fig. 4-7 is twice as high as in Fig. 4-5. The disadvantage is that on-resistance is also doubled, as is obvious from Figs. 4-8 and 4-6. A method of improving on-resistance is described in the following section.

(2) How to reduce on-resistance in basic circuit

On-resistance (or saturation voltage) can be reduced by performing level shift of the Q_2 gate potential in the positive direction. This can be accomplished, for instance, by the methods shown in Fig. 4-9. Fig. 4-10 shows the output characteristics for a case where the gate is level-shifted to the positive side. (14 V is the maximum allowable gate-to-source voltage.)

In the circuit shown in Fig. 4-9, as in the basic circuit, the equivalent drain to source breakdown voltage is twice as high as when a single device is used.

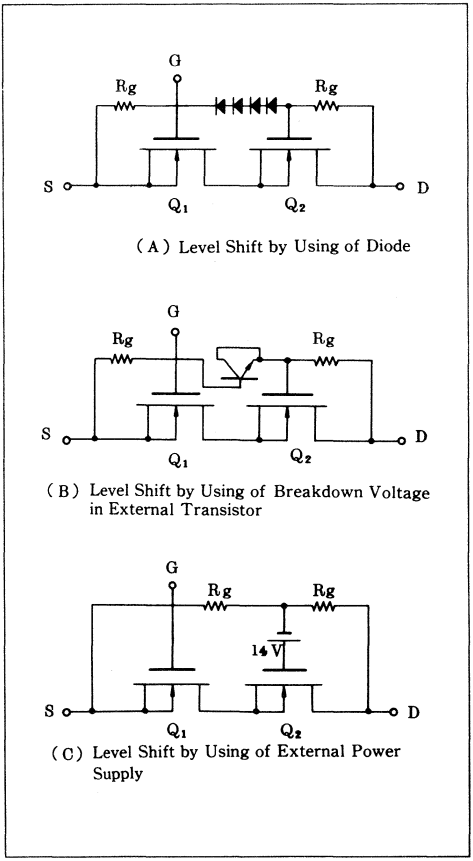
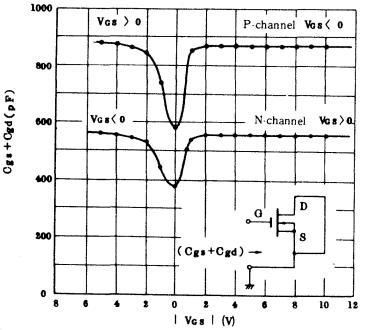


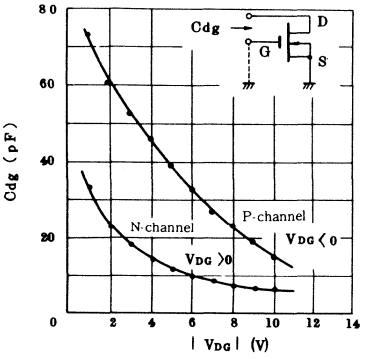
Fig.4-9 How to Reduce ON—Resistance

5.3 Input/Output Capacitance

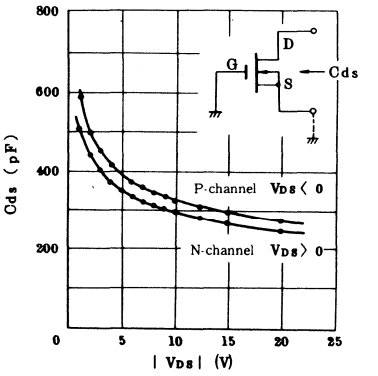
Fig. 5-3 (a), (b'), (c) show the voltage dependence of electrode-to-electrode capacitance of power MOS FETs.



(a) Gate to Source Capacitance + Gate to Drain Capacitance



(b) Drain to Gate Capacitance



(c) Drain to Substrate Capacitance

Fig. 5-3 Bias Voltage Dependencies of Capacitance (2SK135/2SJ50)

Function		Application
Wide band linear amplification		• Audio power amplifiers* • Deflection circuits for CRT displays • Medium wave – high frequency band modulators, transmitters* • Citizen band transmitters
Power switching		• DC-AC inverters • AC-AC converters • DC-DC converters* • General-purpose switching regulators* • Pulse motor drivers
Power oscillation	Power application	• Humidifiers, cleaners and other ultrasonic applications* • High-frequency heaters*
	High voltage application	• Lighting equipment and other high frequency, high efficiency applications • Dischargers, air cleaners*
High-speed switching		• Laser pulsers • Modulators and drivers in high power transmitter circuits for optical communication • Bubble memory drivers
Other		• Series regulators

* Explained in detail in the following section.

8.1 Audio Power Amplifiers

(1) Basic design philosophy

• Frequency characteristics (frequency vs. gain, phase)

The output stage of an ordinary power amplifier uses a push-pull emitter follower (source follower). This method is popular because it provides a wider transfer bandwidth and more stable operation than other grounding systems.

Meanwhile, the forward transconductance (forward transfer admittance) y_{fs} of power MOS FETs is as large as 1.0 S (siemens). Yet it is only a fraction of that of general bipolar transistors and this represents a disadvantage in terms of open loop distortion. The reason is that when bipolar transistors are used as an emitter follower, y_{fs} is given as:

$$y_{fs} = 1/r_e = \frac{I_E}{KT/q}$$

where r_e = Emitter equivalent resistance
K = Boltzmann constant
T = Absolute temperature
q = Electron charge
I_E = Emitter bias current
R_L = Load resistance

Even when I_E is 1 A, for instance, $y_{fs} \doteqdot 40$ S.

Now the relationship between input and output is

$$e_o/e_i = \frac{R_L}{R_L + 1/y_{fs}}$$

and the nonlinier component of y_{fs} causes distortion, so that a larger y_{fs} is of greater advantage. In other words, since a power MOS FET has a distortion about 20 dB larger than a bipolar transistor, it is necessary to use a larger open loop gain and a larger negative feedback than a bipolar transistor. As shown by the frequency characteristics in Fig. 3-4, however, a Darlingoton connection must be used for bipolar transistors in order to enlarge the bandwidth, so that the two-stage emitter follower would worsen the phase characteristics. In applying a negative feedback, a large phase shift would force a sacrifice of gain frequency characteristics in a phase compensation circuit and the like. Thus, with a source follower with a single power MOS FET, much feedback can be applied over a large bandwidth, and distortion can be reduced.

The driver stage of a power MOS FET does not require a conventional class B driver stage. Therefore, the poles in the amplifier system can be reduced and a stable negative feedback amplifier can be formed.

In the frequency characteristics of open loop gain, setting the peak value near 10 ~ 20 kHz is the key to forming a good circuit.

Setting the peak value at the upper limit of the audible range is impossible with conventional bipolar transistors. This can be realized only by using power MOS FETs with excellent high-frequency and switching characteristics.

Fig. 8-1 shows the difference in open loop gain of audio amplifiers designed with power MOS FETs and bipolar transistors.

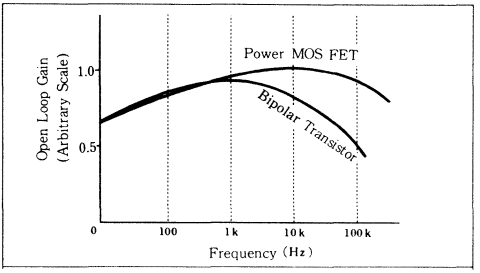


Fig.8-1 Open Loop Gain of Audio Power Amplifier

• Consideration for parastic oscillation

As power MOS FETs have excellent high-frequency characteristics, they are liable to cause oscillation when used in high-gain designs such as described in the preceding section. To avoid this, a gate resistance (200 ~ 500 Ω) may be used to prevent a real part of the input impedance to be negative. Or the gate wiring pattern may be minimized (within 5 cm), as stated in the section on precautions in fabrication later in this manual. Or one-point grounding may be used.

When a gate resistance is inserted, frequency characteristics are worsened as shown in Fig. 8-2, so that optimum values must be selected in designing. The gate resistance will have no effect in case the former stage has a high impedance as in a class A driver stage.

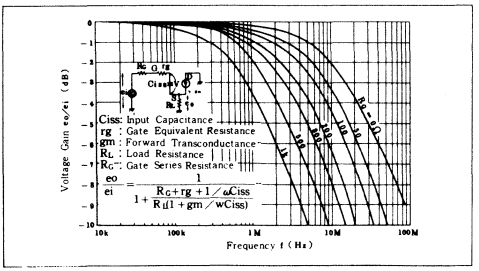


Fig.8-2 Frequeney Characteristies of Source Follower (Calculated Value)

(2) Typical design – 1 (100 W output at 100 kHz, 0.01%)

A circuit is shown in Fig. 8-3. Design of each amplifier stage will be discussed below.

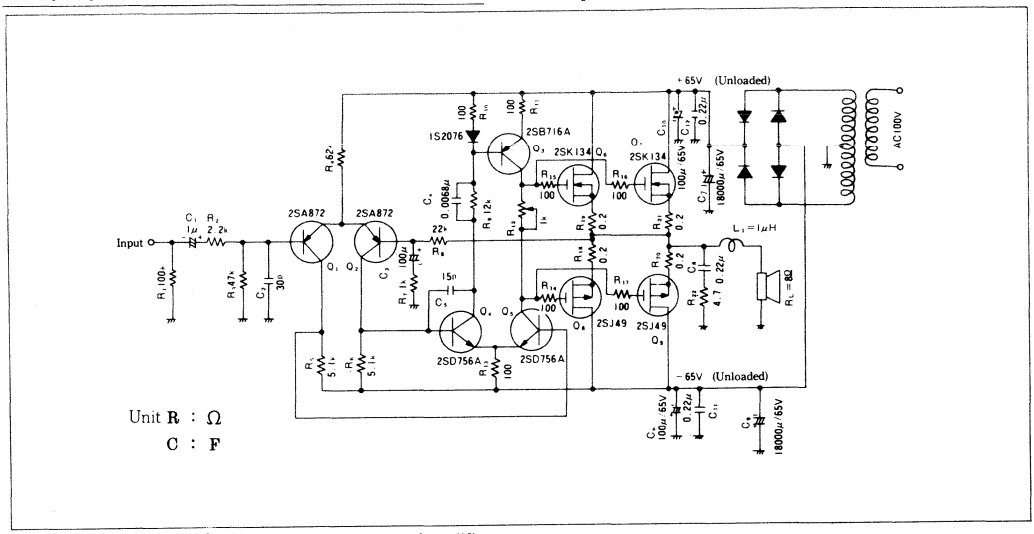


Fig.8-3 Full Circuit of 100 W Output Audio Amplifier

- **Design of output stage**

Fig. 8-4 shows an equivalent circuit of the output stage for N channel MOS FETs. R_{ON} is a drain-to-source equivalent resistance when the power MOS FET is on. The resistance 1.71Ω contains some margin as it was calculated for the worst case from the specifications for 2SK135 and 2SJ50.

$$R_{ON} = \frac{V_{DS(sat)}}{I_D} = \frac{12}{7} \fallingdotseq 1.71\ (\Omega)$$

Peak current I_p flowing in load R_L = 8 Ω at P_O = 100 W is calculated from mean current I,

$$P_O = I^2 \cdot R_L\ ,\ I_p = \sqrt{2} \cdot I,$$

$$\text{as } I_p = \sqrt{2} \cdot \sqrt{\frac{P_O}{R_L}} = \sqrt{2} \cdot \sqrt{\frac{100}{8}} \fallingdotseq 5\ \text{A}.$$

Therefore, if transformer regulation is estimated as 20% and AC line regulation as ±15%, then power supply voltage V_{DD} is given as

$$V_{DD} = 1.2 \times 1.15\ \{R_L + 0.5\ (R_{ON} + R_S)\} \times I_p \fallingdotseq 61.8\text{V}.$$

In Fig. 8-3, the voltage is set at ±65 V including a margin.

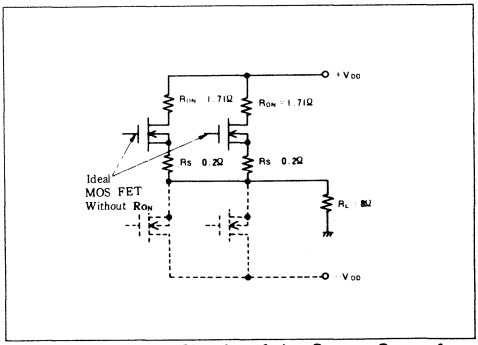


Fig.8-4 Equivalent Circuit of the Output Stage for N-Channel Power MOS FETs

- **Design of voltage amplifier stage**

A power MOS FET can be used with a low driving power. Fundamentally, only the power for charging and discharging the gate-to-source capacitance is needed to the output stage, so that no class B driver stage is required.

The driving power varies with input frequency. At 100 W output and 10 kHz frequency, it would be about 10 mW.

Therefore, an output stage power MOS FET can be driven directly from a class A predriver (voltage amplifier stage) used in a bipolar transistor amplifier. By eliminating the class B driver, the number of components can be reduced, and impairing the amplifier's performance caused by the driver itself can be avoided. Further, the number of poles for transfer function (open loop gain vs. frequency characteristics) decrease, and the stagger can easily be increased. Consequently, the stability against oscillation is improved.

Transistors for the voltage amplifier stage are required to have a high voltage durability, low C_{ob}, and high f_T. Here the 2SD756A/2SB716A developed especially for power MOS FETs are used. With the NPN differential amplifier and PNP constant current load, high gain and low distortion characteristics were obtained.

The class A stage bias current is set as 10 mA. When bias current is lacking, sufficient power to drive a power MOS FET at high frequency cannot be supplied, and distortion would worsen.

The drain current temperature coefficient of a power MOS FET undergoes a reversal of polarity at around I_D = 100 mA and temperature compensation in the large current region will be unnecessary. Hence, the bias circuit for a power MOS FET is vastly simplified because only one semifixed resistor (1 kΩ) for setting idling current will suffice.

- **Design of input stage circuit**

For the input stage, a stable differential amplifier circuit was formed by using the high-voltage, low-noise transistor 2SA872, which is known for its high performance in improving the S/N ratio. Bias current is set as 0.5 mA.

- **Typical characteristics of experimental circuit (Fig. 8-3)**

Output vs. distortion characteristics are shown in Fig. 8-5. At f = 1 kHz, total harmonic distortion (THD) is approximately 0.002%, which is the limit value for any measuring system available on the market today.

Through optimum design, the following can be obtained at rated output:

f = DC ~ 100 kHz,

THD ≦ 0.01%

Thus, characteristics that cannot be obtained with conventional bipolar transistors are realized with power MOS FETs.

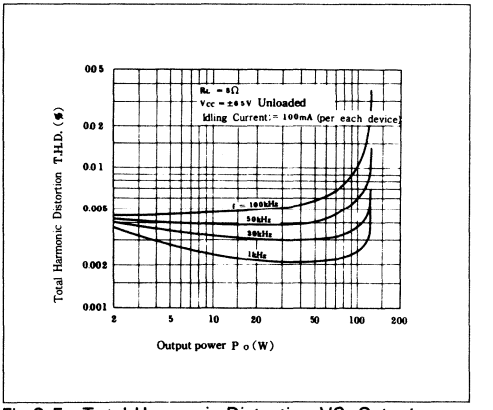


Fig.8-5 Total Harmonic Distortion VS. Output Characteristics

- **Precautions in fabrication**

o Minimize the gate wiring, although its relationship with gate resistance must be taken into consideration.

o Provide one-point grounding for the amplifier base plate, power supply, chemical fapacitor to prevent ± line unbalance, and speaker terminals.

o The output coupling coil has the effect of reducing distortion in the high frequency range, and preventing abnormal oscillation in capacitance loaded operation. But the values should be determined while experimenting.

(3) Typical design – 2 (50 W output at 50 kHz, 0.01%)

Introduced here is a power amplifier with a rated output of 50 W and which attains a total harmonic distortion of 0.01% over the entire frequency bandwidth of from 5 Hz to 50 kHz. The basic design method has been introduced in the previous section. The output stage, as shown in Fig. 8-6, is of the single push-pull construction. Considering the power supply voltage and transformer regulation, the complementary pair 2SK133/2SJ48 would suffice as the power MOS FETs to be used.

This circuit can produce an output of about 70 W by improving transformer regulation or stabilizing the power supply line.

In the frequency characteristics of open loop gain, the peak point is set at 10 kHz, 100 dB. Even at 100 kHz, a high gain of 85 dB is ensured.

Fig. 8-7 shows the distortion vs. output characteristics with the experimental circuit.

In this high negative feedback amplifier, caution must be taken to avoid the oscillation which depends on the printed pattern.

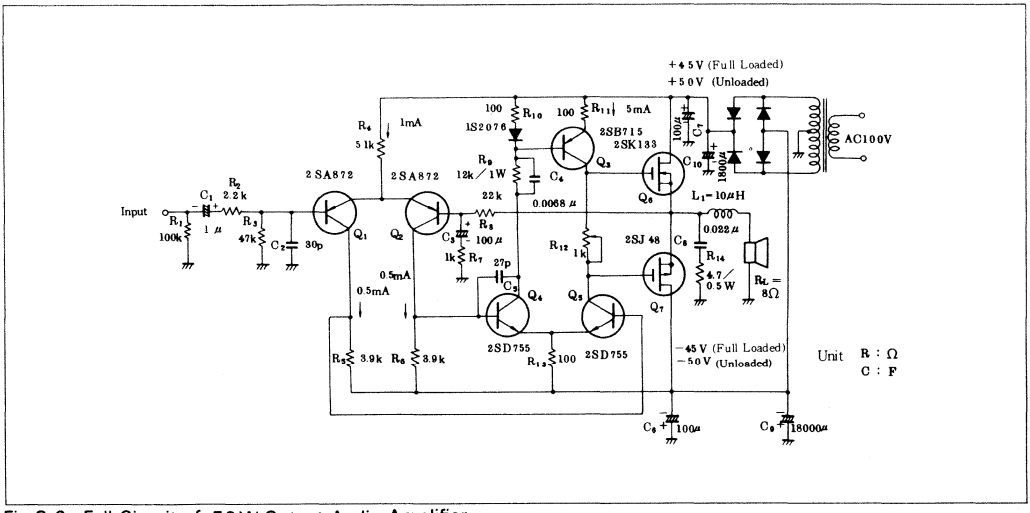


Fig.8-6 Full Circuit of 50W Output Audio Amplifier

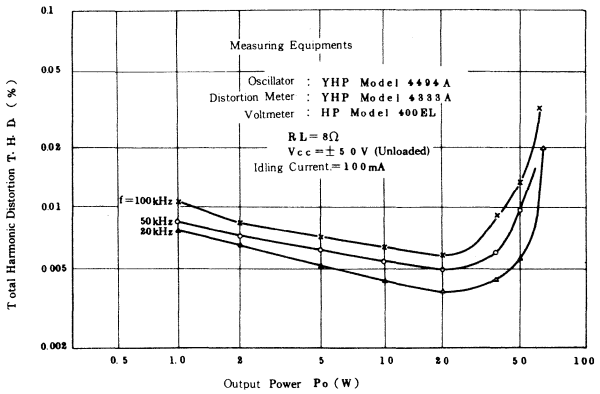


Fig.8-7 Total Hormonic Distortion vs. Output Characteristics

Fig. 8-8 shows the standard printed pattern. The amplifier devices that drive the output stage power MOS FETs consist only of five small-signal transistors, so that the printed board is extremely small.

Wiring between the voltage amplifier stage collector and the power MOS FET gate must be minimized. The arrangement and configuration of the printed board and the heat sink must be selected carefully.

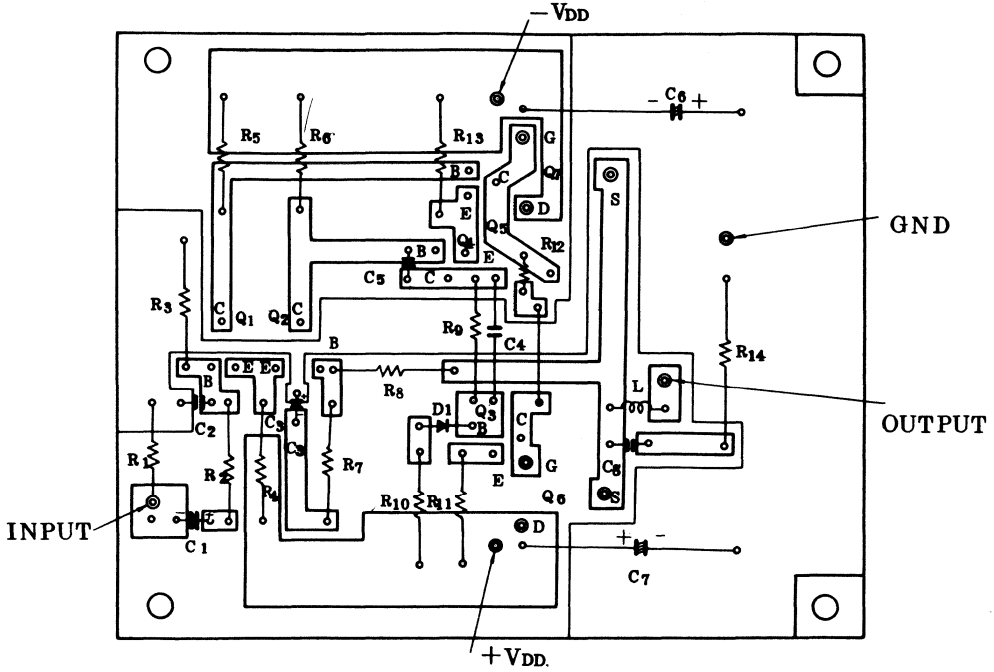


Fig.8-8 Standard Printed Pattern in Actual Size

In Fig. 8-8 which shows the example of the printed board pattern, the printed board is attached directly to the heat sink to minimize the gate wiring.

(4) Recommended line-up by output power

Line-up of devices in audio amplifiers of different outputs is shown Table 8-1.

Table 8-1 Line-up of Devices in Audio Power Amplifier

Output Power (W)	Input Stage		Driver Stage		Output Stage					V_{DSX} (V)
	N-Channel (NPN)	P-Channel (PNP)	N-Channel (NPN)	P-Channel (PNP)	Connection	TO-3		HPAK		
						N-Channel	P-Channel	N-Channel	P-Channel	
50~80	2SK151 (TO-92MOD.)	2SJ51 (TO-92MOD.)	2SK213 (TO-220AB)	2SJ76 (TO-220AB)	Single Push-Pull	2SK133	2SJ48	2SK225	2SJ81	120
	2SC1775 (TO-92)	2SA872 (TO-92)	2SD756 (TO-92MOD.)	2SB716 (TO-92MOD.)						
			2SD756A (TO-92MOD.)	2SB716A (TO-92MOD.)		2SK134	2SJ49	2SK226	2SJ82	140
			2SK214 (TO-220AB)	2SJ77 (TO-220AB)						
100~140	2SC1775 (TO-92)	2SA872 (TO-92)	2SD758 (TO-202AA MOD.)	2SB718 (TO-202AA MOD.)		2SK175	2SJ55	–	–	180
			2SK216 (TO-220AB)	2SJ79 (TO-220AB)						
			2SD666A (TO-92MOD.)	2SB646A (TO-92MOD.)	Parallel Push-Pull	2SK134	2SJ49	2SK226	2SJ82	140
			2SK214 (TO-220AB)	2SJ77 (TO-220AB)						
			2SD668A (TO-126MOD.)	2SB648A (TO-126MOD.)		2SK135	2SJ50	2SK227	2SJ83	160
			2SK215 (TO-220AB)	2SJ78 (TO-220AB)						
150~200	2SC1775A (TO-92)	2SA872A (TO-92)	2SD758 (TO-202AA MOD.)	2SB718 (TO-202AA MOD.)		2SK176	2SJ56	–	–	200

8.2 Power Oscillators (I)

Power MOS FETs have excellent high frequency characteristics and their operating frequency extends to the 10 MHz band and higher. Taking advantage of their high switching speed and ease of biasing, one can use them for economical high-frequency power sources as in such new application as high-frequency heating and high voltage generation.

Power MOS FETs require a far lower driving power than bipolar transistors do, and can be parallel-operated easily, providing the required large output. Basic design procedures for an oscillation circuit and practical applications will be described below.

(1) Basic design of power oscillation circuit

Operation in a high frequency circuit is affected by slight capacitances of the devices and parts used. Also, depending on the DC bias circuit arrangement and ground points, feedback quantity varies and affects the characteristics. Therefore, a circuit configuration determined through calculations must be modified in the process on construction. Described below are the basic principles that provide design guidelines for high frequency FET oscillation circuits.

In Fig. 8-9, (a) is a basic oscillation circuit, and (b) an equivalent circuit. Z_1, Z_2 and Z form a tank circuit. By using the same type of reactance for Z_1 and Z_2, positive feedback can be applied. The signal applied to the gate is amplified at the drain with a 180° phase differential and current of the same phase flows in reactances Z_1 and Z_2, so that it will have a 180° phase differential against the source current. As a result the amplified signal at the gate is positively fed back.

When power MOS FETs are used in a Colpitts oscillation circuit with Z_1 and Z_2 as capacitances, operation at high frequency becomes possible.

Limitation for high frequency operation is created by losses expressed by electrode capacitance C_{gs} and series gate resistance R_g in Fig. 8-9. The voltage applied to the gate is divided between R_g and C_{gs}, and reduces g_m at high frequency. At the same time, phase delay is caused.

The frequency at which g_m decreases by about 3 dB is, in the case of 2SK135:

$$f_{(3dB)} = \frac{1}{2\pi \cdot R_g \cdot C_{gs}}$$

$$\simeq 3 \text{ MHz}$$

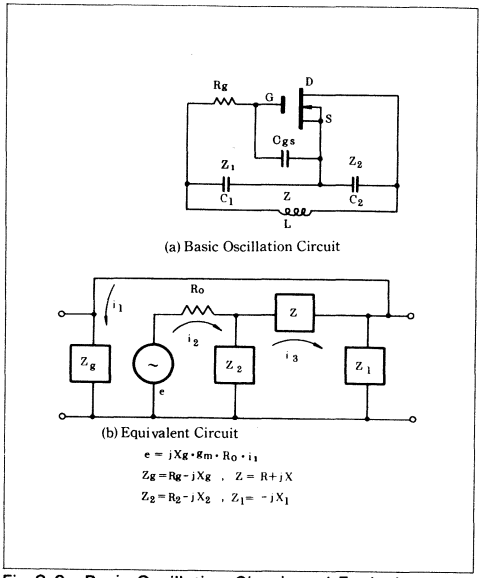


Fig.8-9 Basic Oscillation Circuit and Equivalent Circuit by Using a Power MOS FET

- **Oscillating conditions**

Since power MOS FETs have a large g_m and power gain, an oscillator can be formed even at frequencies higher than $f_{(3dB)}$.

Next, oscillating conditions will be sought for Fig. 8-9 (b).

When gate current is denoted by i_1, drain current by i_2, and tank circuit current including load by i_3, the following equation holds for the loop current:

$$\left.\begin{aligned} &-jXg \cdot g_m \cdot R_o \cdot i_1 + \\ &\quad (R_o + Z_2)\, i_2 - Z_2 \cdot i_3 = 0 \\ &Z_1 \cdot i_1 + Z_2 \cdot i_2 - (Z_2 + Z + Z_1)\, i_3 = 0 \\ &(Z_1 + Z_g)\, i_1 - Z_1 \cdot i_3 = 0 \end{aligned}\right\} \quad \cdots\cdots (1)$$

Equation (1) has finite solutions other than $i_1=i_2=i_3=0$. In other words, in order that the circuit may oscillate, it is necessary that the value of the determinant consisting of constants be zero, as follows:

$$\begin{aligned} &Z_2 \left(jXg \cdot g_m \cdot R_o + Z_2 \cdot \frac{Z_1 + Z_g}{Z_1}\right) \\ &\quad - (R_o + Z_2) \left\{ Z_1 + \right. \\ &\quad \left. (Z_2 + Z + Z_1) \frac{Z_1 + Z_g}{Z_1} \right\} = 0 \end{aligned} \quad \cdots\cdots (2)$$

In an area of operation where drain current i_2 is not dependent on drain voltage but rather on gate voltage, R_O is far larger than the other parameters and the following equation holds:

$$jZ_2 \cdot X_g \cdot g_m + Z_1 - (Z_2 + Z + Z_1)\frac{Z_1 + Z_g}{Z_1} = 0 \quad \cdots\cdots (3)$$

The imaginary part is:

$$R_2 \cdot X_1 \cdot X_g \cdot g_m - (R_2 + R) R_g + (X_2 - X)(X_1 + X_g) + X_1 \cdot X_g = 0 \quad \cdots\cdots (4)$$

If the terms with load resistances R_2 and R of the oscillator are neglected, then frequency would be determined by the following equation:

$$X = \frac{X_1 \cdot Xg}{X_1 + Xg} + X_2 \quad \cdots\cdots (5)$$

Thus,

$$\boxed{(2\pi f)^2 = \omega^2 = \frac{1}{L}\left(\frac{1}{C_1 + Cg} + \frac{1}{C_2}\right)} \quad \cdots\cdots (6)$$

Next, from the real part, we get:

$$X_2 \cdot Xg \cdot gm - (R_2 + R)\frac{X_1 + Xg}{X_1} - (X_2 - X + X_1)\frac{Rg}{X_1} = 0 \quad \cdots\cdots (7)$$

$$gm - \frac{(R_2 + R)}{X_2^2} \cdot \frac{X_2}{X_1 \cdot Xg/(X_1 + Xg)} - \frac{Rg}{Xg^2} \cdot \frac{X_1 \cdot Xg}{X_1 + Xg} \cdot \frac{1}{X_2} = 0 \quad \cdots\cdots (8)$$

From Equation (8), since g_m must be large enough to compensate for circuit loss, the following oscillation start conditions are obtained:

$$gm \geqq \frac{C_2}{Cg + C_1} \cdot Gin + \frac{Cg + C_1}{C_2} \cdot G_L \quad \cdots\cdots (9)$$

Where G_{in} and G_L are loss conductances of input and output circuits respectively.

$$Gin \geqq \frac{Rg}{Xg^2},\ G_L \geqq \frac{R_2 + R}{X_2^2}$$

In the case of high-efficiency power oscillators, the second term on the right side of Equation (9) represents an important loss term, and g_m is expressed with gate voltage V_g, output voltage V_{out}, and output power P_{out}, as follows:

$$gm \geqq \frac{Vout}{Vg} \cdot G_L = \frac{2 \cdot Pout}{Vg \cdot Vout} \quad \cdots\cdots (10)$$

- **DC bias conditions and AC amplitude**

Let us consider the relationship between DC bias conditions and AC amplitude in the various operating modes of the power oscillator in Fig. 8-10.

At conductor angle θ, the various current and voltage parameters of the device are as shown in Fig. 8.11. Drain current is:

$$i_D = I_A (\cos \omega t - \cos \varphi) \quad \cdots\cdots (11)$$

Basic wave amplitude:

$$I = \frac{2}{\pi} \cdot \int_0^{\varphi} i_D \cos \omega t d(\omega t) = I_A \cdot \frac{\varphi - \sin\varphi \cdot \cos\varphi}{\pi} \quad \cdots\cdots (12)$$

Mean current:

$$I_O = \frac{1}{\pi} \cdot \int_0^{\varphi} i_D d(\omega t) = I_A \cdot \frac{\sin\varphi - \varphi \cos\varphi}{\pi} \quad \cdots\cdots (13)$$

The relationship with peak current: $I_p = I_A (1 - \cos \varphi)$

$$I = I_p \cdot \frac{\varphi - \sin\varphi \cdot \cos\varphi}{\pi(1 - \cos\varphi)} \quad \cdots\cdots (14)$$

$$I_O = I_p \cdot \frac{\sin\varphi - \varphi \cos\varphi}{\pi(1 - \cos\varphi)} \quad \cdots\cdots (15)$$

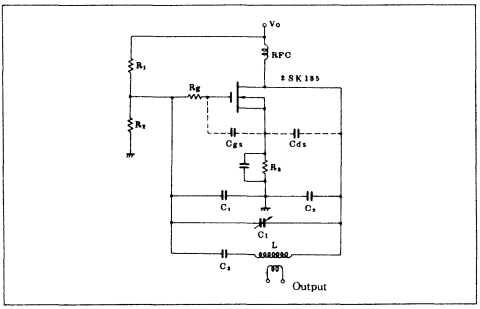


Fig.8-10 Colpitts Oscillation Circuit(Clap-Type)

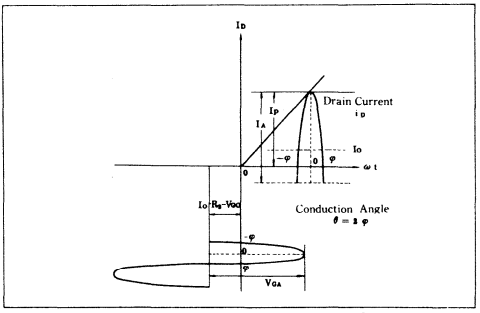


Fig.8-11 Operating Mode of Power Oscillator

The ratio of maximum power against supplied DC power, viz., drain efficiency, is expressed as follows, where current and voltage efficiencies are denoted by η_i and η_e respectively:

$$\eta_D = \eta_e \cdot \eta_i, \qquad \eta_e = \frac{V}{V_O}$$

$$\eta_i = \frac{1}{2} \cdot \frac{I}{I_o} = \frac{1}{2} \cdot \frac{\varphi - \sin\varphi \cdot \cos\varphi}{\sin\varphi - \varphi \cos\varphi} \quad \cdots\cdots (16)$$

η_e can be calculated similarly.

The relationship between conduction angle θ and η_i is given as in Fig. 8-12.

Next, the bias conditions that determine conduction angle $\theta = 2\varphi$ will be sought.

If peak gate voltage is denoted by V_{GP} then:

$$V_{GP} = V_{GO} + V_{GA} - R_3 \cdot I_O \quad \cdots\cdots (17)$$

where $V_{GO} = V_O \cdot \frac{R_2}{R_1 + R_2}$: Initial bias voltage to gate

V_{GA} : Gate amplitude

I_O : Drain mean current

R_3 : Source resistance

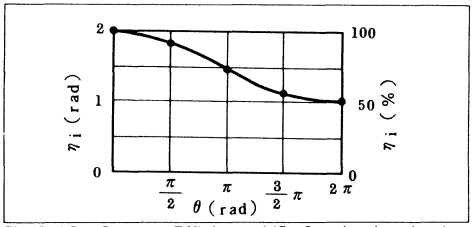


Fig.8-12 Current Efficiency VS. Conduction Angle

If the gate voltage satisfying the conditions for oscillation start is

$$V_{GST} = V_{GO} - R_3 \cdot I_{ST} \quad \cdots\cdots (18)$$

then, from Fig. 8-11, we get

$$V_{GA} \cdot \cos\varphi = R_3 \cdot I_O - V_{GO} \quad \cdots\cdots (19)$$

From Equations (17), (18), (19), we get:

$$R_3 = \frac{V_{GST} + \frac{\cos\varphi}{1 - \cos\varphi} \cdot V_{GP}}{I_O - I_{ST}} \quad \cdots\cdots (20)$$

$$V_{GO} = V_{GST} + R_3 \cdot I_{ST} \quad \cdots\cdots (21)$$

$$V_{GA} = \frac{V_{GP}}{1 - \cos\varphi} \quad \cdots\cdots (22)$$

- **Determination of circuit parameters**

Circuit parameters and maximum ratings of devices for an FET oscillator will be considered. For high-efficiency operation, drain bias voltage must be maximized. Let us make it one-half the allowable voltage V_{DSX} max. of the device.

$$V_O = \frac{1}{2} V_{DSmax} \quad \cdots\cdots (23)$$

From the relationship between allowable drain loss and mean voltage, we get the drain mean current as follows:

$$I_O = \frac{P_D}{V_O} \quad \cdots\cdots (24)$$

Equation (24) represents a condition where allowable loss is not exceeded even at oscillation stop.

The peak current for class B operation is obtained from Equation (15) as follows:

$$I_P = \pi \cdot I_O \quad \cdots\cdots (25)$$

Gate peak voltage V_{GP} can be determined as a value corresponding to I_p in Equation (25) from the I_D - V_{DS} characteristics of power MOS FETs (see Figs. 3-1 and 3-2 in Chapter 3). As for oscillation starting current I_{st}, from the conditions of Equation (10), denoting drain voltage amplitude by V, the following is determined:

$$gm > \frac{2 \cdot Pout}{Vg \cdot V} \fallingdotseq \frac{2 \cdot Io \cdot \eta_p}{Vg} \quad \cdots\cdots (26)$$

For safety's sake, the value of oscillation start current is determined from the g_m - I_D characteristics of power MOS FETs (see Fig. 8-13) as the value of I_{st} corresponding to twice the value of Equation (26). From these data and Equations (20), (21) and (22), the bias parameters of V_{GO} and V_{GA} can be determined.

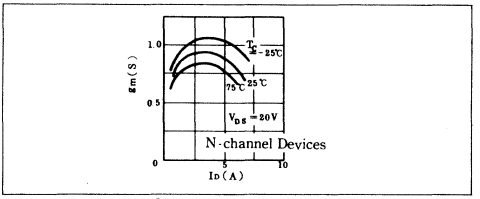


Fig.8-13 Drain Current Dependency of Transconductance

- **Example of parameter calculation**

By applying the above method to 2SK135, the following calculated results are obtained:

V_O = 70 (V)
I_O = 1.43 (A)
I_p = 4.5 (A)
V_{GP} = 6 (V)
g_m = 2 x 0.374 (S)
I_{st} = 0.6 (A)
V_{GO} = 2.9 (V)
V_{GA} = V_{GP} = 6 (V)

- **Calculation of resonator capacitance**

In order to set the divided voltages of gate voltage V_g (= V_{GA}) and drain voltage V_D to meet the above operating conditions, resonator capacitances C_1 and C_2 will be determined.

With regard to drive voltage drop due to R_g, the following equation holds:

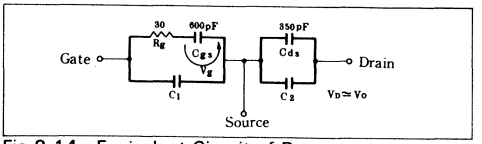


Fig.8-14 Equivalent Circuit of Resonator

$$\frac{Vg}{V_D} = \frac{Cds + C_2}{Cgs + C_1} \cdot \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_0})^2}} \quad \cdots\cdots (27)$$

where $\omega_0 = \frac{1}{Rg \cdot Cgs}$

And the values of capacitance pair C_1 and C_2 are determined. Coil inductance for the desired frequency can be derived from these capacitance values.

The value of load Q can be increased by using a Clappe type oscillator in which a capacitance is provided in parallel between the gate and drain or inserted in series with the inductance.

The load is expressed as follows, using output voltage V_{out} and circuit efficiency η_C.

$$P_{out} = P_{DC} \cdot \eta_D \cdot \eta_C = \frac{1}{2} \cdot \frac{V_{out}^2}{R_L} \quad \cdots\cdots (28)$$

The specified output can be obtained by giving a resistance or output voltage satisfying Equation (28).

This oscillator gives the maximum output at optimum load but no destruction of devices occurs even under overload. In other words, gate driving voltage is proportional to drain voltage and, under light load, drain voltage does not exceed bias voltage. Under heavy load, drain voltage amplitude decreases and the power MOS FET is protected.

(2) Experimental circuit and typical characteristics (13.5 MHz, 40 W)

When the constants are determined in accordance with the basic design procedure described in item (1) above, the circuit shown in Fig. 8-15 is obtained. The circuit configuration is extremely simplified and can be applied to circuits that give the desired frequency and output power.

Fig. 8-16 shows the supply voltage dependency of major characteristics. An outstanding feature is that high-efficiency oscillation is obtained because circuit efficiency does not change with supply voltage or output power.

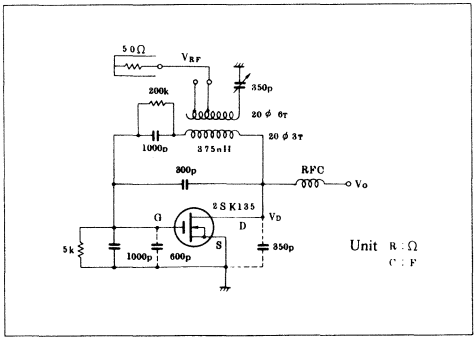


Fig.8-15 Source-Common Type Oscillator (Class-AB Operation)

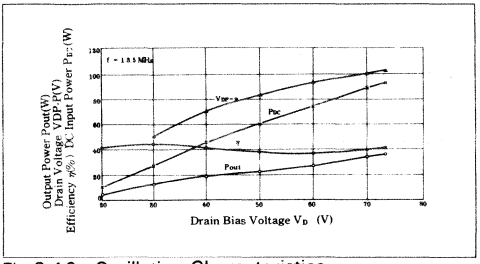


Fig.8-16 Oscillation Characteristics

8.3 Power Oscillators (II) (DC-DC Inverter)

The inverter described here introduces the basic theory of the Colpitts oscillator referred to above in order to obtain high frequency and high power, so that it can be applied to high-frequency, high-efficiency lighting equipment, dischargers, and air cleaners. Important performance requirements for inverters and converters are as follows:

- High power efficiency (small circuit losses).
- Large area of safe operation for power devices and minimal temperature rises for equipment.
- Low spike noise at switching of power devices and stable output.
- Little unnecessary radiation from equipment.
- Small weight and volume of equipment.

The above requirements vary in importance depending on the system in which inverters and converters are used. But indispensable performances of power devices are exactly those which Hitachi's power MOS FETs feature, namely:

- High switching speed.
- Simple driving circuit; large power gain so that driving power may be minimized.
- Large current handling capability in the area of safe operation, particularly in the high voltage area (secondary breakdown region), because these devices are used at high voltage.

• Typical design

With 400 ~ 500 V output voltage and 400 kHz frequency as the target specifications for the inverter, circuit constants will be determined.

For deriving output, a capacitor loaded in the middle of the oscillator loop will be used. Output current will thus be obtained by discharge of electrons accumulated in the capacitor.

First the basic circuit is set as in Fig. 8-17, where C_L denotes a load capacitor, R_1 and R_2 are bias resistances of gate, and V_i stands for unstabilized input voltage (which gives V_G and V_D).

Fig. 8-18 plots output voltage and frequency with C_1 as parameter under the conditions of $C_1'=\infty$, C_2 = 0.05μF, L = 0.0384mH, C_S = 5 pF, R_E = 2Ω, C_E = 0.1μF, C_L = Open, R_2 = 70 kΩ, V_i = 45V.

The figure shows that output voltage is dependent on the C_1 value and there is an optimum output voltage. Oscillation frequency also varies with C_1 and shows a tendency of monotone increase and decrease.

Next, characteristics measured with input voltage Vi as parameter are shown in Fig. 8-19. The measurement conditions are $C_1'=\infty$, C_2 = 0.05 μF, C_S = 5 pF, R_E = 2Ω, C_E = 0.1μF, C_L = Open, R_2 = 70 kΩ.

Fig. 8-19 shows that the desired output voltage is dependent on input Vi and can be selected at will and that frequency variation can be reduced. Frequency drift during operation is due to heat generation in the capacitor. For practical purposes, a low-loss capacitor with a small temperature coefficient (e.g., mica, polypropylene) must be used.

The inverter introduced above involves a relatively small power. But a similar principle applies to high-voltage power supplies that require higher frequencies and higher voltages.

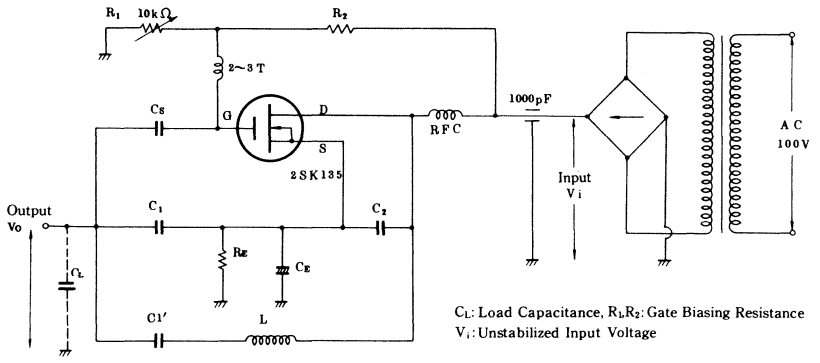


Fig.8-17 Basic Inverter Circuit

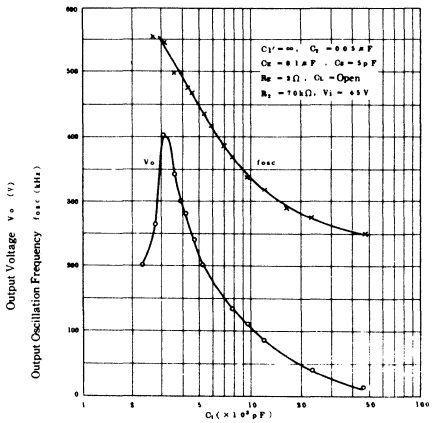


Fig.8-18 Vo, fosc - C_1 Characteristics

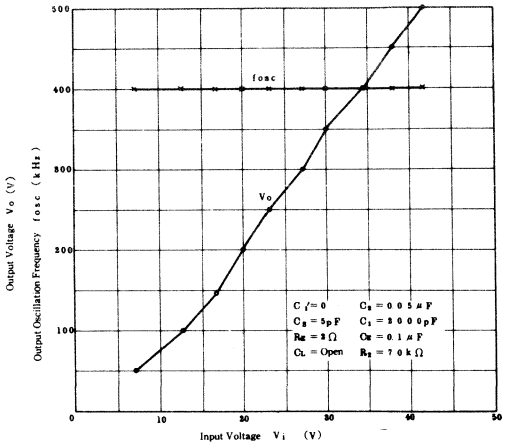


Fig.8-19 Vo, fosc - Vi Characteristics

8.4 Medium-Wave Transmitters (Based on data of NHK Technical Research Laboratories)

Solid state devices are being used increasingly nowadays in medium-wave transmitters. However, no optimum power devices are available for use in power amplifier circuits and not a few problems involving circuit performance remain to be resolved. A high-efficiency, high-power pulse amplifier using power MOS FETs will be described.

Generally, in pulse amplification, power MOS FETs have many advantages over bipolar transistors, as follows:

- Pulse width does not change because of the absence of carrier storage effect.
- Drain current has a negative temperature coefficient, so that no thermal runaway or current hogging occurs; as a result, stable operation is ensured.
- They have a large input resistance; since they are enhancement type devices, input and output terminals are isolated and the bias circuit is simplified compared with other field effect transistors.
- A small driving power suffices; driver and input power amplifier circuits are simplified.
- The desired output is obtained easily by parallel operation.
- Design, adjustment and operation are simple.

A class D SEPP pulse amplifier with 1 kW CW at 0.5 ~ 1.5 MHz carrier frequency and 80 ~ 90% overall efficiency will be described. A class D type is selected because a final power amplifier efficiency of 90% or better can be expected theoretically.

(1) Class D SEPP type pulse amplifier

Fig. 8-20 is a block diagram of the power amplifier.

In the carrier generator, radio frequency is pulse-width-modulated by the audio frequency signal. Here, pulse-width-modulated wave is generated according to the two-valued logic, and is drawn out as two-phase pulse and applied to the driver stage.

The input parts of the power amplifier are transformer coupled. Amplitude modulation wave is mixed and filtered in the output tank circuit and applied to the load (antenna).

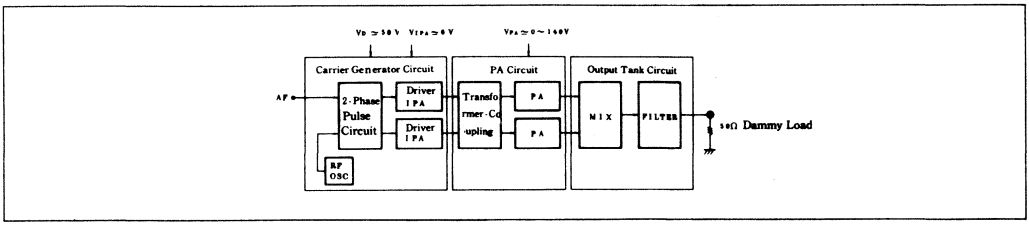


Fig.8-20 Block Diagram of SEPP Pulse Power Amplifier

- **Power amplifier circuit**

Fig. 8-21 shows a power amplifier circuit. A total of 16 power MOS FETs are used, four each in parallel.

In the SEPP system, since the source electrodes of power supply side MOS FETs Q_1 and Q_1' are connected to the output transformer, an AC coupling system with capacitors and resistors cannot be used. A transformer coupling as shown in Fig. 8-21 is required.

The primary and secondary winding ratio of the input transformer is 1 : 1 (5 turns each) and bifiler winding is used. An E type core is used, but output characteristics vary considerably with the kind of core.

A clock pulse of 140 $V_{P\text{-}P}$, which is the maximum rated voltage for this device, is applied to the gate of the PA stage power MOS FET.

Fig. 8-22 shows theoretical waveforms at different points in Fig. 8-21. Since only carrier signals are used in this case, only the unmodulated carrier component is obtained at the output terminal.

When a pulse-width-modulated wave is applied as a clock pulse to the MOS FET gate, a two-valued PWM wave (1 level: V_{PA}, -1 level: $-V_{PA}$) that has undergone pulse-width modulation with audio frequency is obtained at the output transformer secondary. This PWM wave is filtered in the series resonance circuit consisting of a choke coil and capacitor, and the basic component is derived. Since the crest value of waveform of this basic component varies with pulse width, only the amplitude modulated wave is derived at the output terminal.

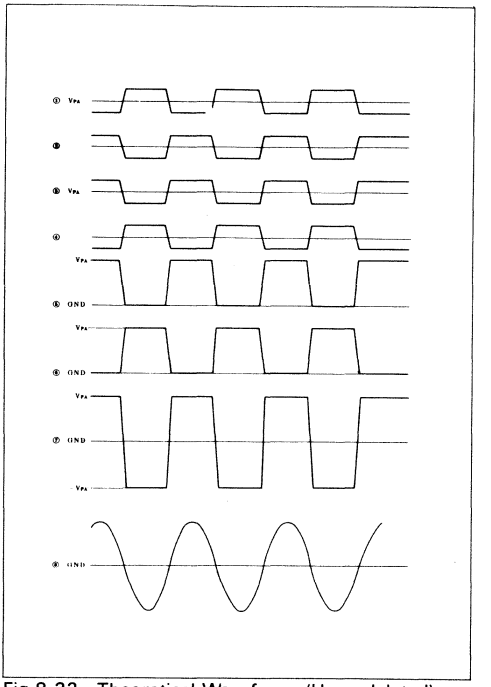


Fig.8-22 Theoretical Waveforms (Unmodulated)

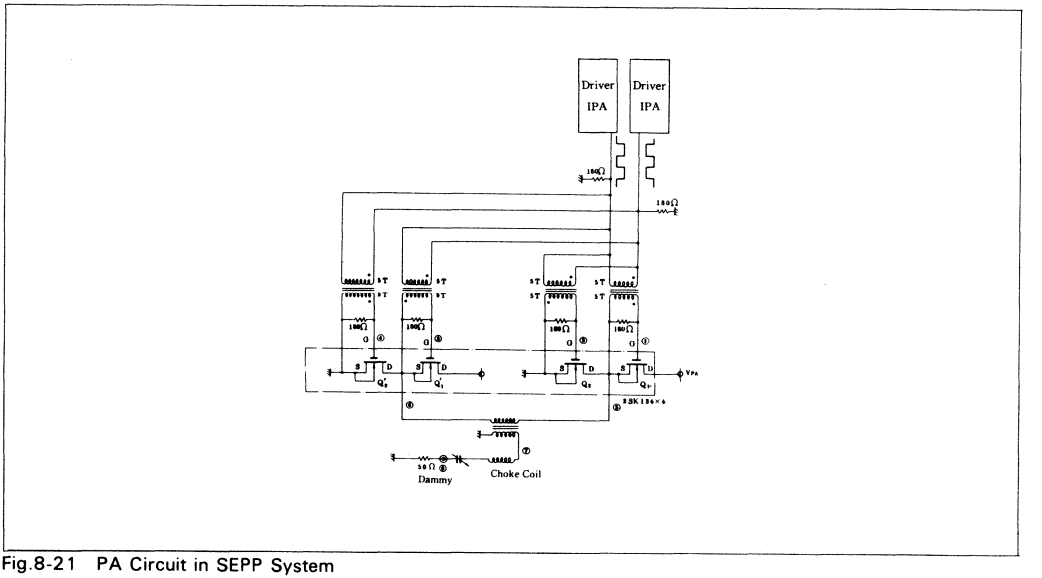


Fig.8-21 PA Circuit in SEPP System

- **Output variation by transformer winding ratio**

Figs. 8-23 through 8-25 show the dependence of output power and power amplifier efficiency on PA supply voltage at different winding ratios. Fig. 8-26 plots the relationship between PA efficiency and output power with winding ratio as the variable.

While no reference will be made here to transformer types (e.g., core shape, bobbin shape), it has been verified experimentally that use of an E type core and a flat bobbin is effective in achieving high efficiency.

The characteristics shown in Fig. 8-23 through 8-25 are the result of optimum selection based on these tendencies.

From these experiments, it is found that an efficiency of 80 ~ 90% can be expected at PA power supply voltages of 0 ~ 140 V, if the output transformer primary vs. secondary winding ratio is selected at below 1 : 4. Particularly at a winding ratio of 1 : 2, stable operation was obtained at 1.3 kW output power (1 MHz continuous wave) and 87% efficiency.

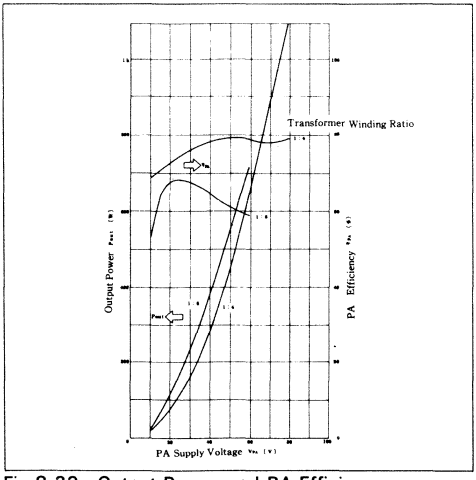


Fig.8-23 Output Power and PA Efficiency vs. PA Supply Voltage for Various winding Ratio of Transformer

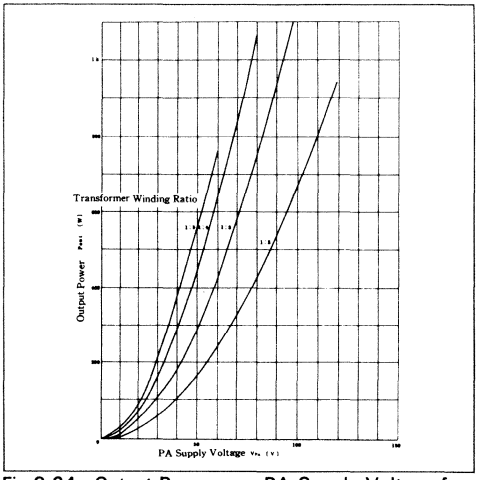


Fig.8-24 Output Power vs. PA Supply Voltage for Various winding Ratio of Transformer

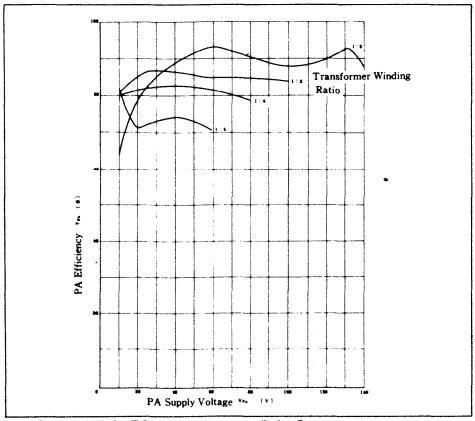


Fig.8-25 PA Efficiency vs. PA Supply Voltage for Various Winding Ratio of Transformer.

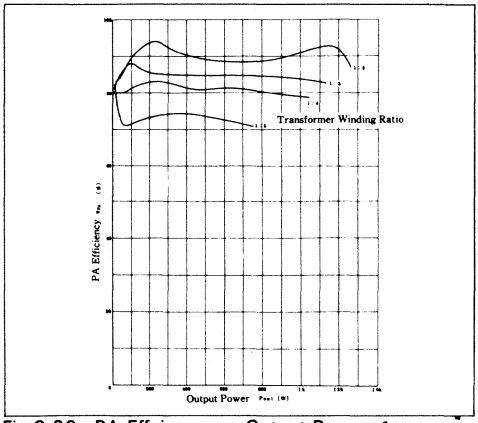


Fig.8-26 PA Effciency vs. Output Power for Various Winding Ratio of Transformer

[Reference Data]

Table 8-1 Various Transformer Types

No.	Winding Ratio	Bobbin	Core
F1	Primary : Secondary = 1:2 (Primary : 8 Turns, Parallel in 5 Secondary : 16 Turns, Parallel in 2) Material : Enamel wire ϕ 2mm	Material: Teflon Refer to Fig. 8-27	Insert H6ER-type Ferrite
F2	Primary : Secondary = 1:4 (Primary : 3 Turns, Parallel in 4 Secondary : 12 Turns, Parallel in 2) Material : Enamel wire ϕ 2 mm	–	E-Core Refer to Fig. 8-28(a)
F3	Primary : Secondary = 1:6 (Primary : 2 Turns, Parallel in 4 Secondary : 12 Turns, Parallel in 2) Material : Enamel wire ϕ 2 mm	–	E-Core Refer to Fig. 8-28(a)
F4	Primary : Secondary = 1:2 (Primary : 2 Turns, Parallel in 4 Secondary : 4 Turns, Parallel in 2) Material : Enamel wire ϕ 2 mm	–	E-Core Refer to Fig. 8-28(b)
F5	Primary : Secondary = 1:3 (Primary : 2 Turns, Parallel in 4 Secondary : 6 Turns, Parallel in 1) Material : Enamel wire ϕ 2 mm	–	E-Core Refer to Fig. 8-28(b)

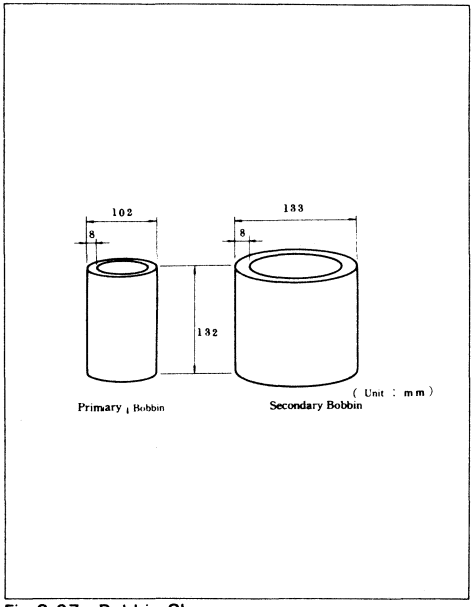


Fig.8-27 Bobbin Shape

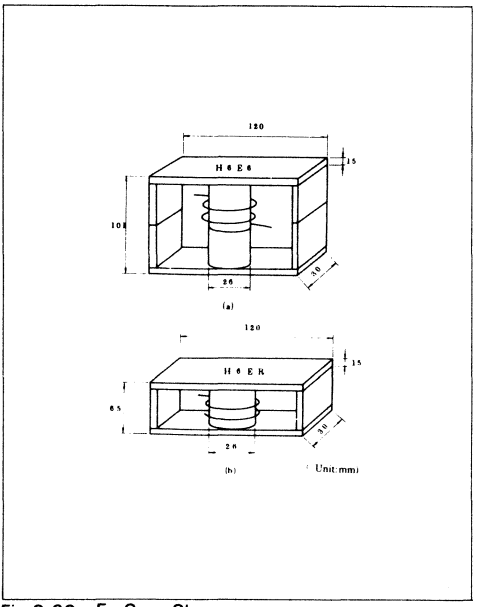


Fig.8-28 E–Core Shape

8.5 High Power Switching Regulators Using Direct Rectification System

Design of a 500 W class switching regulator using power MOS FETs will be introduced. Described below are the features of power MOS FETs as switching devices, followed by calculation of ideal characteristics, design procedure, and measured values.

(1) Advantage of power MOS FETs

Power MOS FETs are capable of high-speed switching, so that the driving circuit is simplified even for frequencies as high as several hundred kHz. Also, when a variable duty ratio control system is used, carrier storage time of the power MOS FET can be neglected, and a wide control range is ensured.

Therefore, output well follows input ripples, and a small filter capacity suffices. This contributes much to improving regulator performance.

Next, switching frequency can be raised to the limit, which is dependent on the performance of the high-speed rectifier diode. Therefore, efficiency can be augmented, equipment can be made compact, and safety improved compared with transistor converters.

(2) Calculation of ideal characteristics

Fig. 8-29 shows a theoretical circuit for a switching regulator. When it is assumed that capacity C is sufficiently large, output E_O is constant, and both switch S and coil L have no loss, then, from the current waveform of Fig. 9-30, the following equilibrium equation holds:

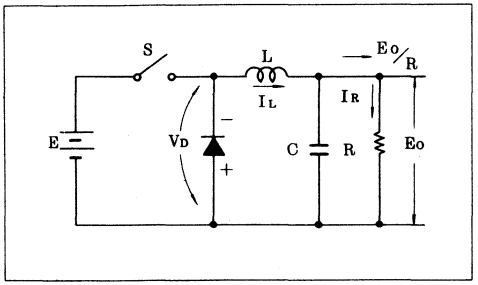


Fig.8-29 Theoretical Circuit for a switching Regulator

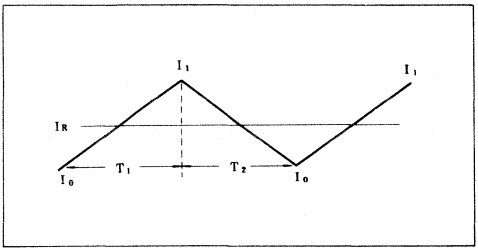


Fig.8-30 Output(Load) Current Waveform

At switch on:

$$L\frac{dI_L}{dt} = E - E_O \quad \cdots\cdots (1)$$

$$\therefore I_L = \frac{E - E_O}{L} \cdot t + I_0 \quad \cdots\cdots (2)$$

$$I_1 = \frac{E - E_O}{L} \cdot T_1 + I_0 \quad \cdots\cdots (3)$$

At switch off:

$$L \cdot \frac{dI_L}{dt} = -(E_O + V_D) \quad \cdots\cdots (4)$$

$$\therefore I_L = -\frac{E_O + V_D}{L} \cdot t + I_1 \quad \cdots\cdots (5)$$

$$I_O = I_1 - \frac{E_O + V_D}{L} \cdot T_2 \quad \cdots\cdots (6)$$

Thus, $(E - E_O)T_1 = (E_O + V_D)T_2$

Therefore, $E_O = E \cdot \frac{T_1}{T} - V_D \cdot \frac{T_2}{T}$ where $T = T_1 + T_2$ $\cdots\cdots (7)$

Mean load current I_R will be:

$$I_R = \frac{I_1 + I_0}{2} \quad \cdots\cdots (8)$$

Next, if I_0, I_1 is denoted by I_R, then

$$I_1 = I_R + \frac{E - E_O}{2 \cdot L} \cdot T_1 \quad \cdots\cdots (9)$$

$$I_0 = I_R - \frac{E - E_O}{2 \cdot L} \cdot T_1 \quad \cdots\cdots (10)$$

Since minimum load current I_0 is larger than 0, from Equation (10), the minimum value for coil L will be:

$$L_{min} = \frac{E - E_O}{2I_R} \cdot T_1 \quad \cdots\cdots (11)$$

If the variation value of load current is put as $\Delta I = I_1 - I_0$, then, from Equations (9) and (10), we get

$$\Delta I = \frac{E - E_O}{L} \cdot T_1 \quad \cdots\cdots (12)$$

If variation ratio is put as $\alpha = \Delta I / I_R$, then the required L value is determined as

$$L = \frac{E - E_O}{\alpha I_R} \cdot T_1 \quad \cdots\cdots (13)$$

To seek conduction angle T_1/T, from Equation (7), we get

$$E_O = E \cdot \frac{T_1}{T} - V_D\left(1 - \frac{T_1}{T}\right)$$

Therefore,

$$\frac{T_1}{T} = \frac{E_O + V_D}{E + V_D} \quad \cdots\cdots (14)$$

Next, let us seek the values of power and efficiency.

$$\text{Input power } W_i = \frac{E}{T}\int_0^{T_1} \left(\frac{E - E_O}{L} \cdot t + I_0\right) dt$$

$$= \frac{E}{T}\left(\frac{E - E_O}{2L} \cdot T_1^2 + I_0 \cdot T_1\right)$$

Substituting Equations (9) and (10) into this, we get

$$W_i = \frac{T_1}{T} \cdot E\left(\frac{I_1 - I_0}{2} + I_0\right)$$

$$= \frac{T_1}{T} \cdot E \cdot I_R = E \cdot \frac{E_O + V_O}{E + V_D} \cdot I_R \quad \cdots\cdots (15)$$

Output power

$$W_O = E_O \cdot I_R \quad \cdots\cdots (16)$$

Output efficiency

$$\eta = \frac{W_O}{W_i} = \frac{E_O}{E} \cdot \frac{E + V_D}{E_O + V_D} \quad \cdots\cdots (17)$$

Power loss W_D of the rectifier diode is given as:

$$W_D = V_D \cdot \frac{1}{T}\int_0^{T_2} \left(I_1 - \frac{E_O + V_D}{L} t\right) dt$$

$$= V_D \cdot \frac{1}{T}\left(I_1 \cdot T_2 - \frac{E_O + V_D}{2L} \cdot T_2^2\right)$$

$$= \frac{V_D}{T}\left(I_1 \cdot T_2 - \frac{I_1 - I_0}{2} \cdot T_2\right) = V_D \cdot I_R \cdot \frac{T_2}{T}$$

$$= V_D \cdot \frac{E - E_O}{E + V_D} \cdot I_R \quad \cdots\cdots (18)$$

$$\text{Thus, } W_i = W_L + W_D = \left(E_O + V_D \cdot \frac{E - E_O}{E + V_D}\right) I_R$$

$$= E \cdot \frac{E_O + V_D}{E + V_D} \cdot I_R \quad \cdots\cdots (19)$$

- **Typical values**

If it is assumed that E = 100 V, E_O = 50 V, W_L = 200 W, V_D = 1V, I_R = 4A, f = 80 kHz (T = 12.5 μs), then T_1 = 6.3μs.

When α = 0.5, then $L = \frac{E - E_O}{0.5\, I_R} \cdot T_1 = 157\ \mu H$,

η = 0.99 (99% efficiency)

Efficiency increases as input, output voltage ratio E_o/E approaches 1.0. In designing an actual switching regulator, losses and optimum values must be calculated individually for the main power supply, switching circuit, control circuit, and filter circuit.

(3) Typical design

- **Basic design philosophy**
- Maximum output 500 W
- Variable voltage range 10 ~ 100 V
- Input power 500 W
- Input voltage 140 V
- Type of circuit Input part is a 100 V AC direct bridge rectification system; power MOS FETs are driven by capacitance-coupling and controlled by variable duty type control.
- Switching frequency 40 kHz (25 μs)
  Rectifier diodes currently available have a reverse breakdown voltage of 300 V, a maximum current of 6 A, a reverse recovery time of 0.2 μs, and a forward voltage of 0.8 V or so. If these performance figures are improved, switching can be performed at higher frequencies.
- The sensing output voltage feedback loop is isolated by a photo coupler.
- Output transformer winding ratio and core 20 : 18 in turns; EIH-90.
- **Cautions in fabrication**
- Since the output transformer winding is subject to sharp current spikes, it is required to have a large capacity. Vinyl wire is recommended.
- Providing a center tap on the output transformer's secondary winding and using full-wave rectification are effective in reducing rectifier diode loss. (In the example described below, the bridge rectification system is used for both primary and secondary windings.
- A large capacity choke coil should be used in order to maintain a constant current over a wide range.
- **Circuit operation**

The basic circuit configuration of this regulator is shown in Fig. 8-31.

In the sensing block, the voltage at the output terminal is divided and compared with the reference voltage generated by a Zener diode, and the error voltage is output.

Here, a single operational amplifier IC, HA17741, is used in the error amplification circuit and the overcurrent limitation circuit. The circuit configuration is a standardized one.

In the control block, a variable duty circuit is used to reduce noise.

The power MOS FET has a switching speed as fast as 20 ~ 30 ns and is liable to generate noise. Also, its high input impedance can induce external noise, which in turn can

cause misoperation.

In the variable duty circuit, therefore, rectangular waves in which the direct current component is superposed on the error signal are integrated and the voltage comparator is operated at the cross-zero point.

As a result, the loop has a low response speed but is not affected by noise.

The drive block uses the CMOS inverter IC HA14011B which drives the power MOS FETs and a complementarily connected 200 mW class transistor. This block illustrates the characteristic ease of use of power MOS FETs. The driver need only have an input power of 10 V and a charge/discharge capacity of 1,000 pF. The drive circuit is vastly simplified. If it is assumed that the power MOS FET rise time t_r is 30 ns, then, one only has to consider the 300 mA transient current and the approximately 0 mA steady state current (there is a slight leak current).

The circuitry of the blocks described above is presented in Figs. 8-32 through 8-34.

Fig. 8-35 shows a timing chart for the control block.

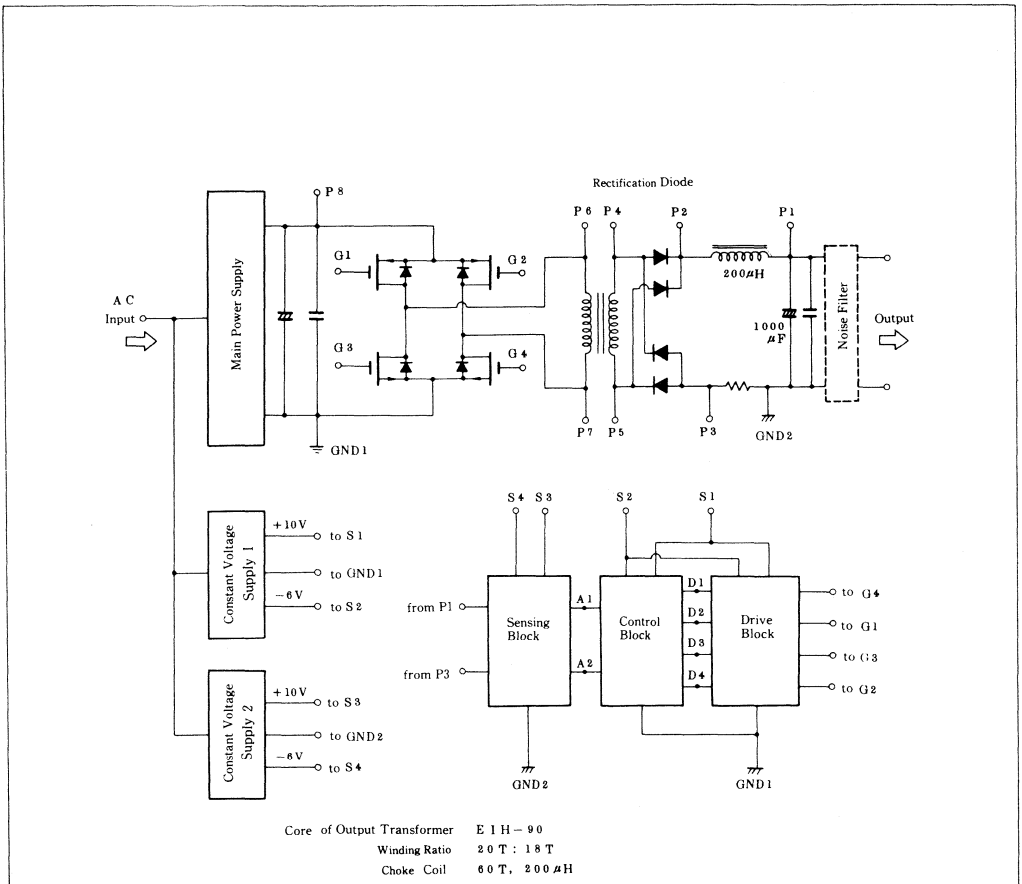


Fig.8-31 Block Diagram of High Power Switching Regulator

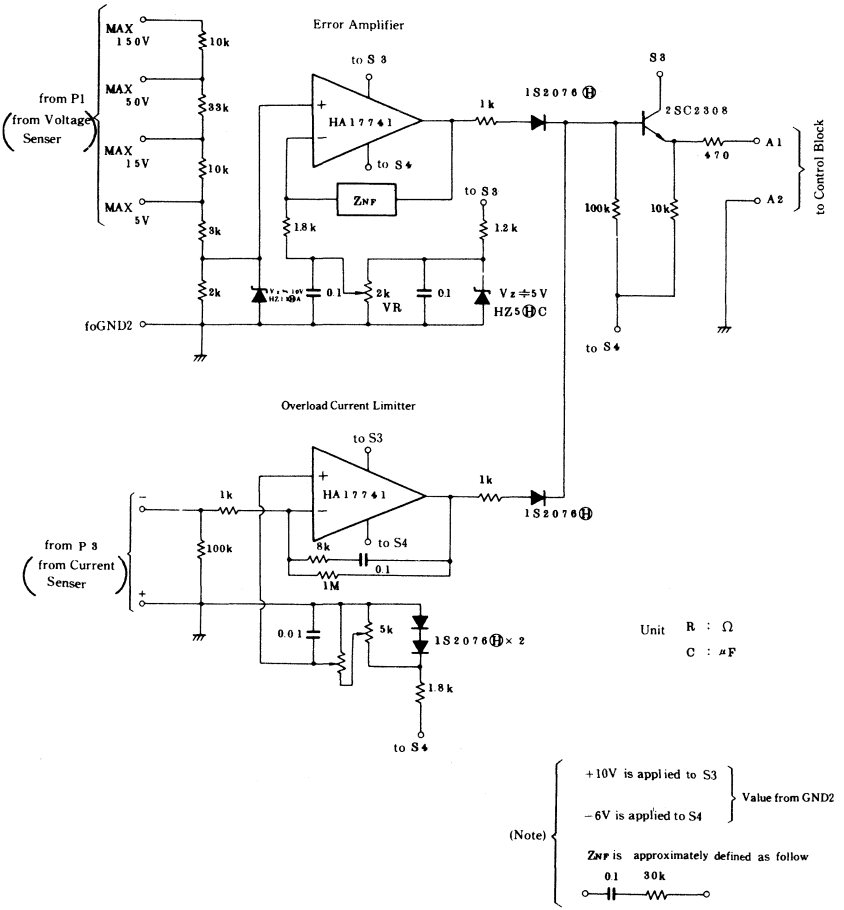
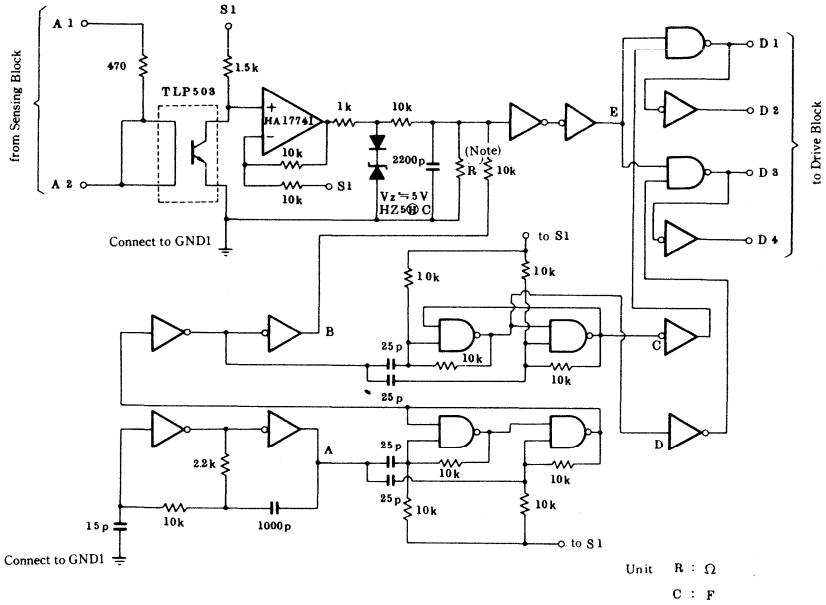
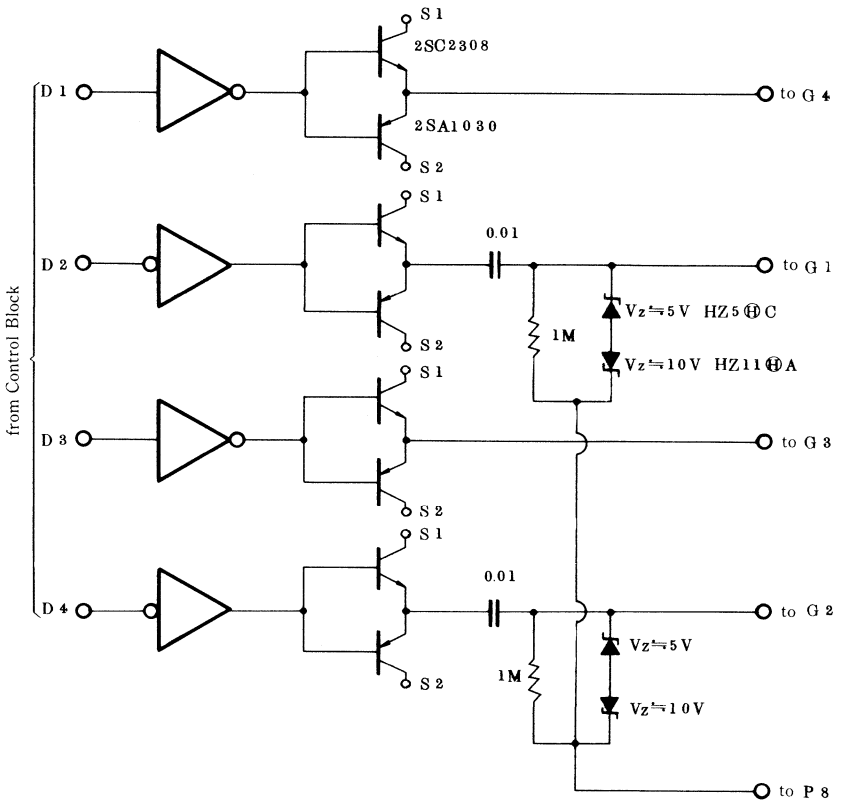


Fig.8-32 Sensing Block



(Note)
- + 10V is applied to S1 / − 10V is appied to S2 } Value from GND1
- HD14011B is used for all gates.
- For the inverter, it is necessary that one gate is pulled-up to S1. (Do not use 2 gate in parallel)
- The supply voltage S1 and S2 should be given to HA17741 and HD14011B
- R must be adjusted to determine the dead time. The value will be approximately 10 kΩ .

Fig.8-33 Control Block



Unit R : Ω
C : μF

(Note)
- For the inverter, HD14011B is used with one gate Pulled-up to S1.
- S1 is +10V, and S2 is −6V. S1 and S2 should be given to V_{DD} and Vss of HD14011B respectively.
- The transistors are 4 pairs of 2SC2308 & 2SA1030.

Fig.8-34 Drive Block

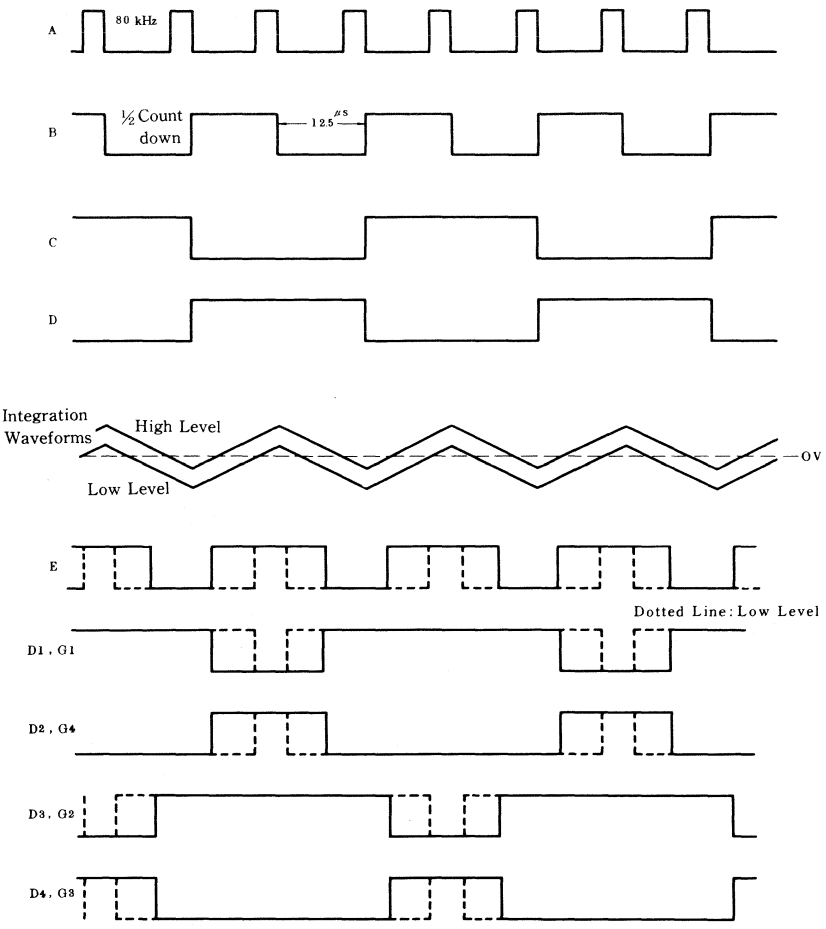


Fig.8-35 Theoretical Waveforms in Control Block

- **Nominal characteristics of experimental circuit**

Figs. 8-36 and 8-37 show voltage waveforms, respectively, for the output transformer secondary and differential voltage between choke coil terminals. It will be seen that the conduction angle follows the specified output. Under the operating conditions of 80 V and 3 A, the duty factor is about 70%. Other characteristics illustrated are the following:

Fig. 8.38 Regulation characteristics

Fig. 8-39 Efficiency vs. output current characteristics (V_O constan

Fig. 8-40 Efficiency vs. output voltage characteristics (I_O constan

Fig. 8-41 Efficiency vs. output current characteristics (P_O constan

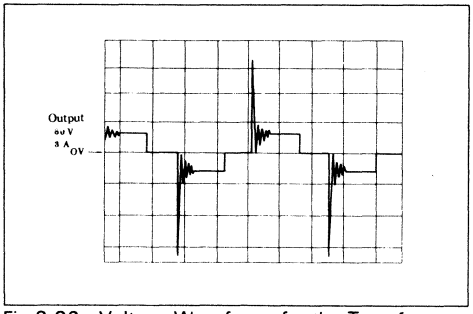


Fig.8-36 Voltage Waveforms for the Transformer Secondary

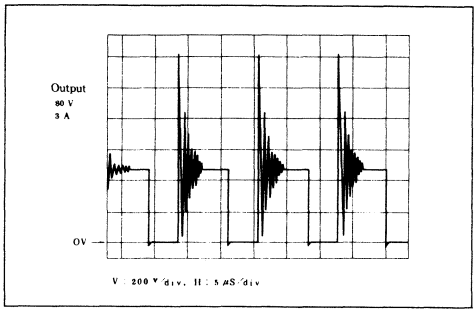


Fig.8-37 Voltage Waveforms for the Differential Voltage between Choke Coil Terminals

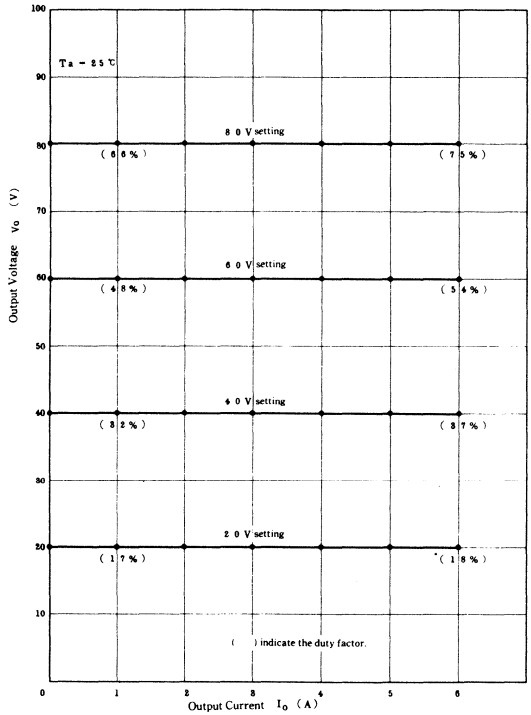


Fig.8-38 Regulation Characteristics

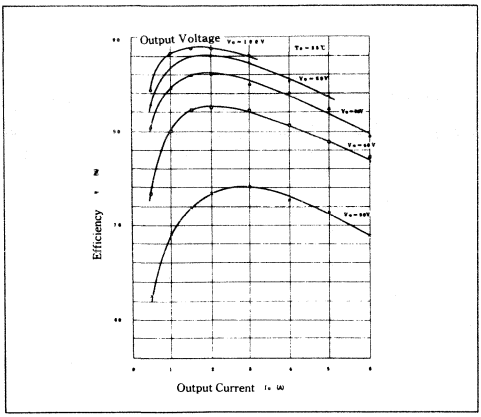


Fig.8-39 Efficiency vs. Output Current Characteristics (Vo constant)

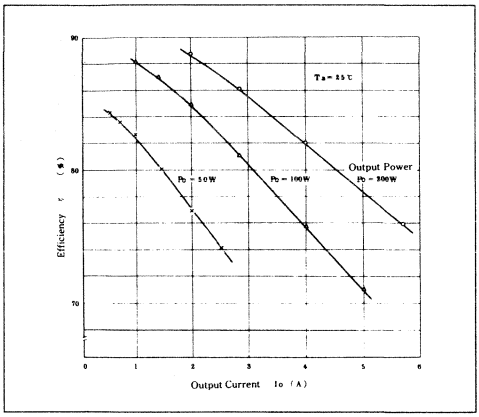


Fig.8-41 Efficiency vs. Output Voltage Chracteristics (Po constant)

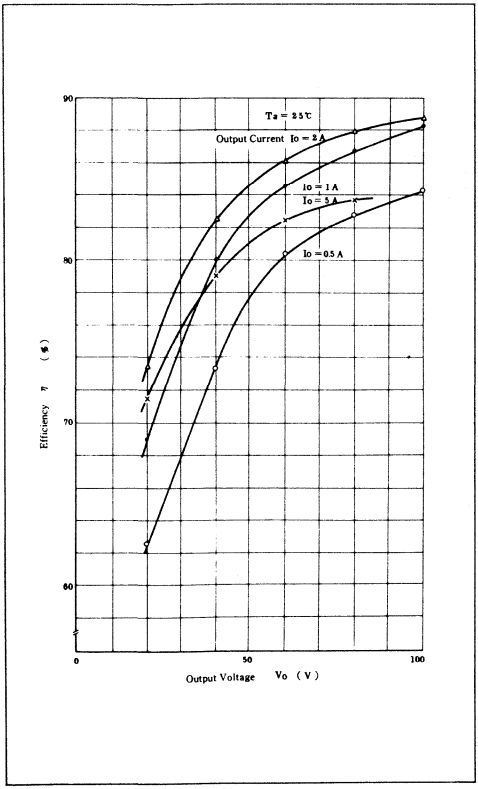


Fig.8-40 Efficiency vs. Output Voltage Characteristics (Io constant)

8.6 Low-Noise DC-DC Converters

The converter introduced here is based on a design philosophy different from that of the high-power, high-efficiency switching regulator described in the preceding chapter.

Spike noise has been reduced to the limit in this converter, so that it can be used in the PCM decoder part of electronic switching systems which are sensitive to noise at the small signal level.

The circuitry and test results are described below.

(1) Circuit configuration and operation

A block diagram is presented in Fig. 8-42. It is a single-transistor converter using a power MOS FET as the main switch. Low noise is achieved by:

- effectively utilizing the electrode structure of power MOS FETs (source electrode is connected to header), and
- loosely coupling the output transformer.

For driving and controlling the power MOS FET, a CMOS gate IC is employed.

A 12 V, 5 mA subsidiary power supply is provided by dividing the voltage at the AC input.

The control loops are isolated by means of a photo coupler of 4 MHz bandwidth.

Radiation can be coped with by a shield plate; there is no need for a special noise filter. (When the converter was mounted in a PCM decoder, crosstalk to the adjacent channel was below –90 dBm/20 kHz.)

Since carrier storage effect can be neglected in driving a power MOS FET, a mirror integration circuit is formed with C_2 and the transformer primary, as shown in Fig. 8-42. As a result, the switching waveform draws a gentle slope and the spike component is completely removed.

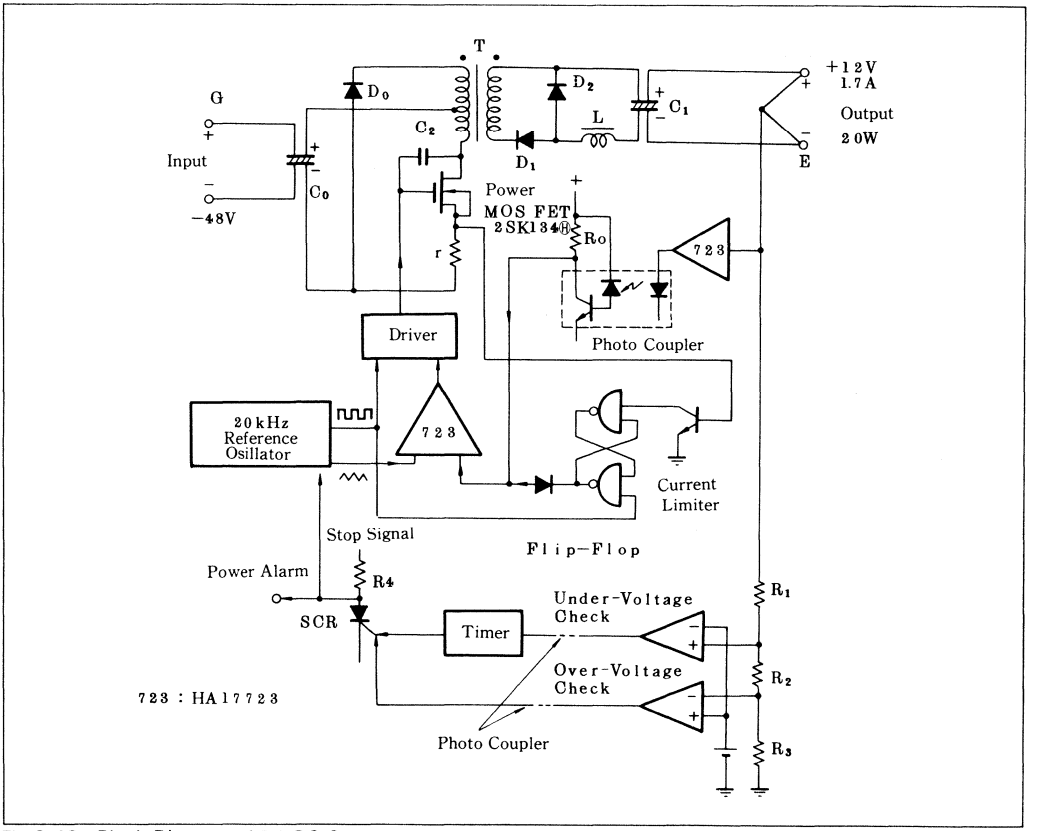


Fig.8-42 Block Diagram of DC-DC Converter

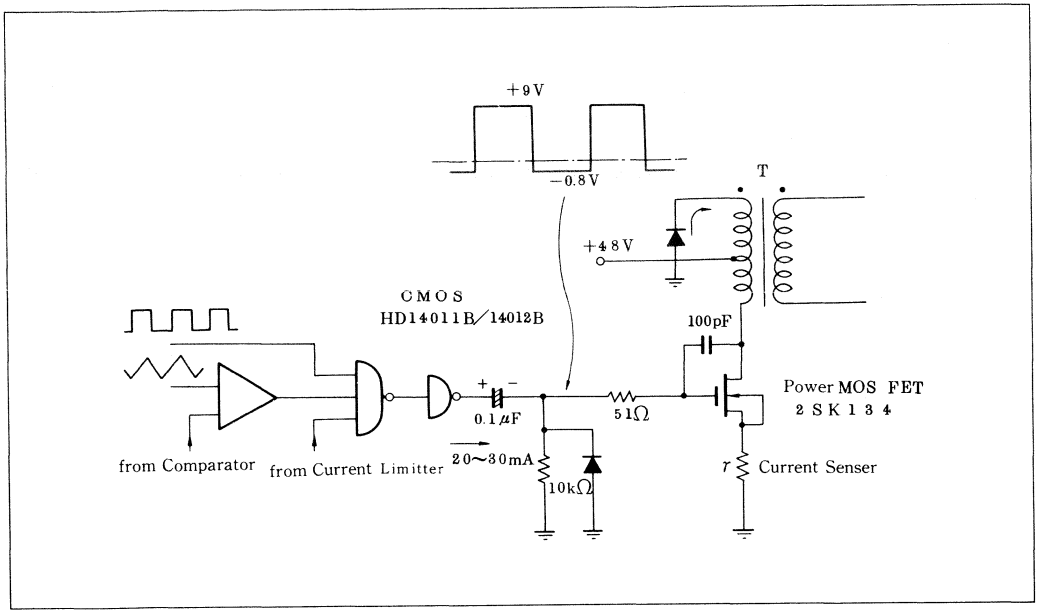


Fig.8-43 Drive Circuit for DC–DC Converter

(2) Results of experiment

Major performance figures are shown in Table 8-2. By taking advantage of the performance, circuits that produce the desired output voltage and current can be designed.

Table 8-2 Major Performance Figures

Item	Condition	Performance
Input Voltage	–	−48±5V
Output Voltage, Current	Full load	+12V, 1.7A
Spike Voltage	Full load	4mVp-p
Regulation for Input Voltage Changes	−48V → −53V	+2mV
Regulation for Load Changes	Non load → Full load	−17mV
Efficiency	Full Load Full Circuit	71%

Figs. 8-44 and 8-45 show operation waveforms of the power MOS FET, and Fig. 8-46 the output terminal ripple and spike noise waveforms.

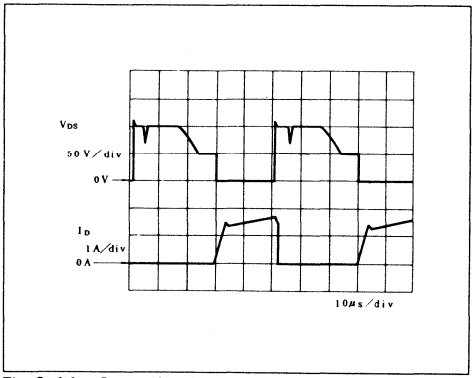


Fig.8-44 Operation Waveforms of Power MOS FET

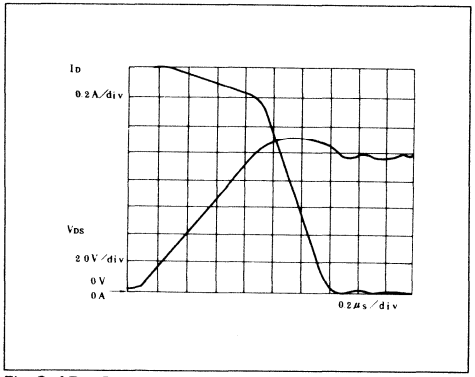


Fig.8-45 Operation Waveforms of Power MOS FET

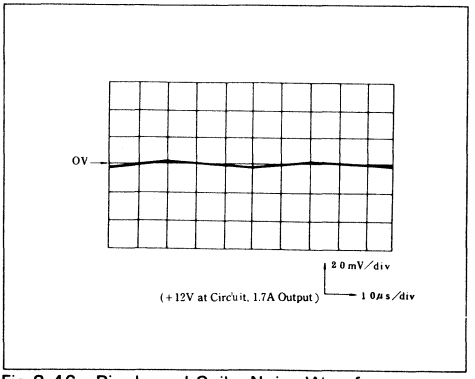


Fig.8-46 Ripple and Spike Noise Waveforms

Interface circuits

Suggested circuits for driving loads using MOS FETS from various logic sources.

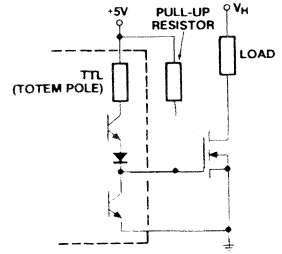


Figure 1. Direct Drive from TTL Output

Table 1. Driving MOS FETs from TTL (Totem Pole Outputs)

Logic Conditions	54/74	54H/74H	(54L)/ 74L	(54LS)/ 74LS	74S
Logic Zero Min. sink current for V_{OL}	16mA ≤0.4V	20mA ≤(0.4V)/	(2)/3.6mA ≤(0.3V)/ 0.4V	(4)/8 ≤(0.4V)/ 0.5V	20mA 0.5V
Logic One Max. source current for V_{OH}	-0.4mA ≥2.4V	-0.5mA ≥2.4V	-0.2mA ≥2.4V	-0.4mA ≥(2.5)/ 2.7V	-1.0mA ≥2.7V
Typical Gate Propagation Delay	10ns	7ns	50ns	12ns	4ns

Table 2. Driving MOS FETs from C-MOS (Buffered)

	Standard Buffered Outputs			4049/4050 Drivers		
Logic Conditions \ Logic Supply Voltage	5V	10V	15V	5V	10V	15V
Logic Zero: Approximate sink current for $V_{OL} \leq 1.5V$	1.5mA	3.5mA	4mA	20mA	40mA	40mA
Logic One: Minimum source current for V_{OH}	-0.51mA ≥4.6V	-1.3mA ≥9.5V	-3.4mA ≥13.5V	-1.25mA ≥2.5V	-1.25mA ≥9.5V	-3.75mA ≥13.5V
Typical switching times of logic drive signals: RISE	100ns	50ns	40ns	100ns	50ns	40ns
FALL	100ns	50ns	40ns	40ns	20ns	15ns

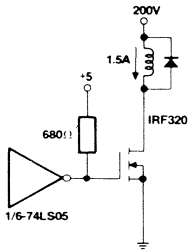


Figure 2. Waveforms Associated with a MOS FET Driven by a TTL Gate

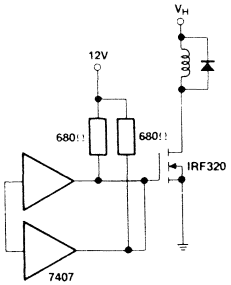


Figure 3. Waveforms Obtained with High Voltage TTL Driver

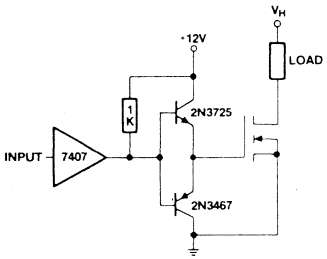


Figure 4. Simple Interface to Drive MOS FETs from TTL

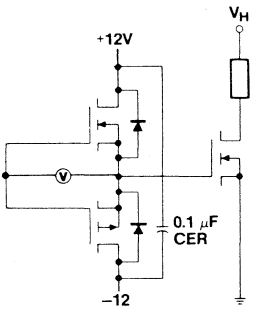
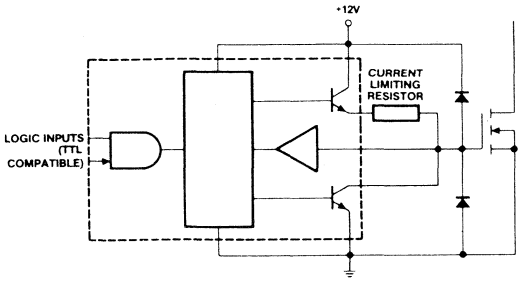


Figure 5. High Performance Driver



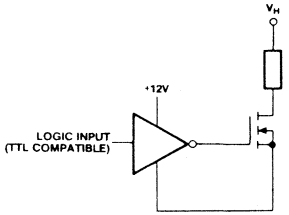


Figure 6. Buffer Stages Implemented with Special Purpose Drivers

Suggested circuits for driving loads using MOS FETS from various logic sources.

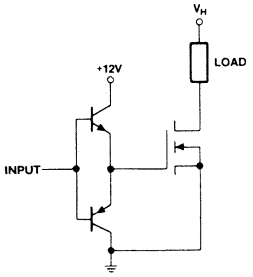


Figure 7 Current Booster for Analog Applications

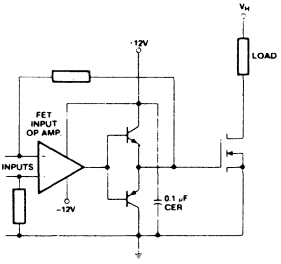


Figure 8 Dual Supply Op-Amp Drive Circuit

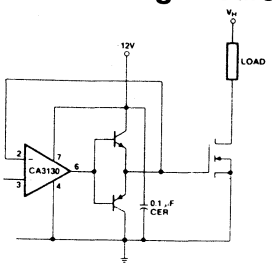


Figure 9 Single Supply Op-Amp Drive Circuit (Voltage Follower)

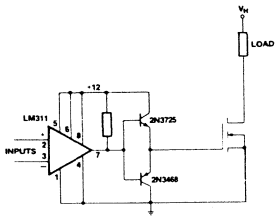
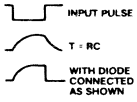


Figure 10 Comparator Drive



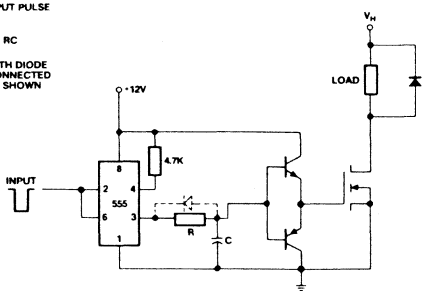


Figure 11 555 as Schmitt Trigger in a Pulse Shaping Application

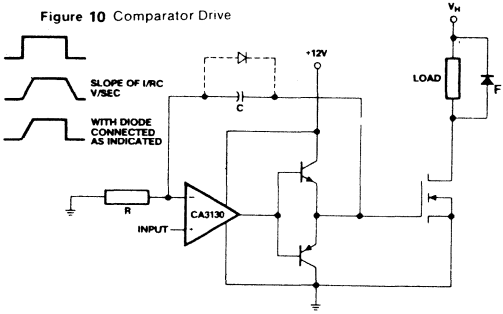


Figure 12 Pulse Shaper

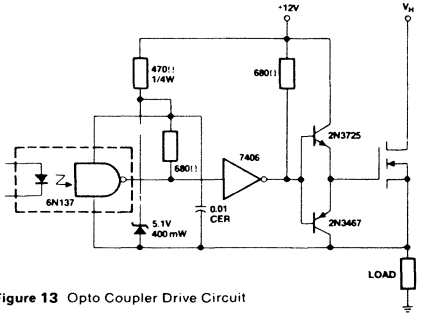


Figure 13 Opto Coupler Drive Circuit

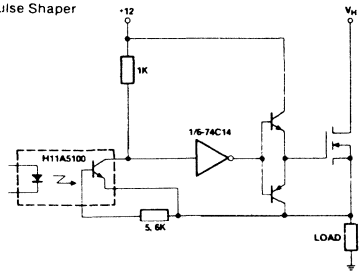


Figure 14 Simplified Opto Coupler Drive.
555 can be substituted for the 74C14

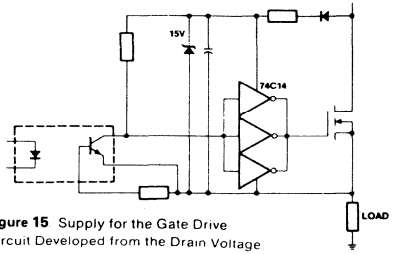


Figure 15 Supply for the Gate Drive Circuit Developed from the Drain Voltage

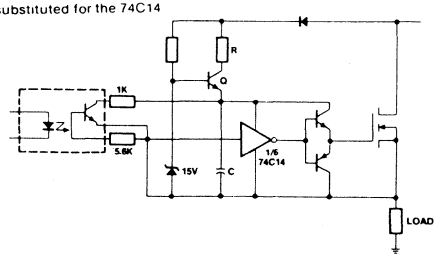


Figure 16 Gate Drive Supply Developed from the Drain Voltage for Small Duty Cycle or Low Frequency Operation

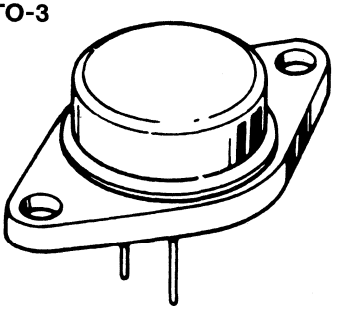
POWER MOS FET Cross Reference

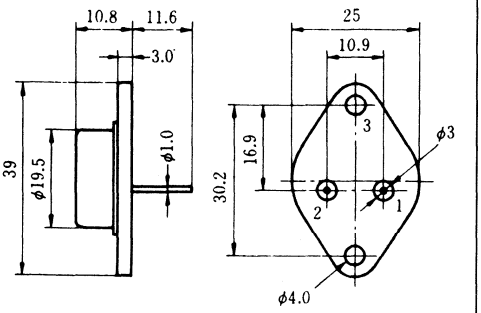
HITACHI TAKASAKI WORKS
DISCRETE SEMICONDUCTOR ENGNG. DEPT.

HITACHI	ABSOLUTE MAX. RATING		PACKAGE	JAPAN		U. S. A.					Europe
	V_{DSS} [V]	I_D [A]		N E C	TOSHIBA	I R C	Motorola	Supertex	Intersil	Siliconix	Siemens
2SK347	400	1	DPAK								
2SK375	300	1				IRF711/713					
2SK384	500	0.3		2SK337(TO-126)							
2SK352	250	0.3	TO-126								
2SK294	80	5	TO-220AB			IRF523/521	MTP814	VNO308N5	IVN5201CND-CNF		
2SK295	100	5		2SK339		IRF520/522	MTP815	VNO309N5			BUZ20
2SK296	300	1				IRF711/713					
2SK310	400	3				IRF722/710		VNO340N5	IVN6000CNS		
2SK311	450	3				IRF821/823		VNO345N5	IVN6000CNT		BUZ40
2SK319	400	5		2SK338		IRF730/732	MTP565				
2SK320	450	5				IRF831/833	MTP474				BUZ41
2SK345	40	5						VN0204N5	IVN5201CND		
2SK346	60	5				IRF521/523	MTP1224	VNO206N5	IVN5201CNE		
2SJ101	-40	-5									
2SJ102	-60	-5				IRF9531/9533					
2SK382	500	2				IRF820/822	MTP475		IVN6000CNU		BUZ40
2SK383	100	10				IRF530/532	MTP1225	VN1209N5			BUZ20
(HS7853)			(TO-3P)								
(HS7854)											
(2SK349)	400	10									
(2SK350)	450	10									
2SK343	140	8	HPAK		2SK272(TO-3P)						
2SK344	160	8				IRF631/633					
2SJ99	-140	-8			2SJ92(TO-3P)						
2SJ100	-160	-8									
(HS7851)	200	8				IRF620/632					
(HS7852)	-200	-8									
2SK258	400	8	TO-3	2SK278		IRF330/332	MTM565	VNO340B1		VN4000A/4001A	
2SK299	450	8				IRF431/433	MTM474	VNO345B1			BUZ44
2SK308	120	10				IRF130-133	MTM1224/1225	VN1208N1		VN64GA	BUZ23
2SK312	400	12			2SK324	IRF352		VNO440N1			
2SK313	450	12			2SK325	IRF453		VNO445N1			BUZ45
2SK351	800	5									BUZ84
HS84033	250	10			2SK356	IRF230					BUZ34
(HS84039)	100	10				IRF132	MTM1034	VN1209N1			BUZ23
(HS84040)	-100	-10				IRF9130					

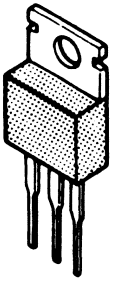
The HITACHI devices are a "form, fit and function" replacement for the indicated type numbers, but subtle differences in characteristics or specifications may exist.

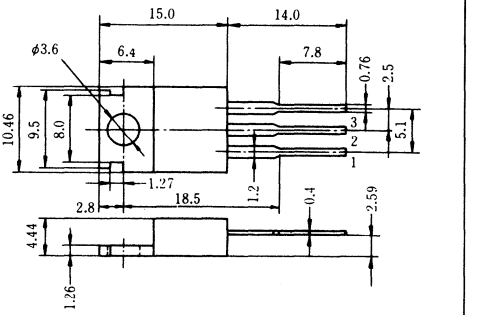
TO-3



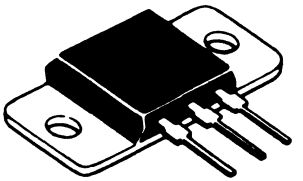


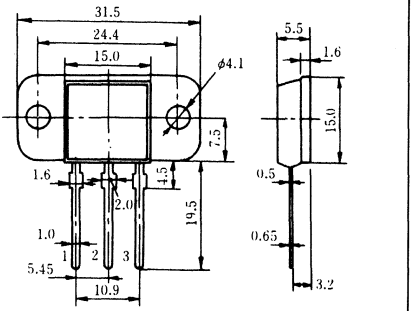
TO-220AB



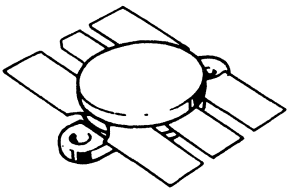


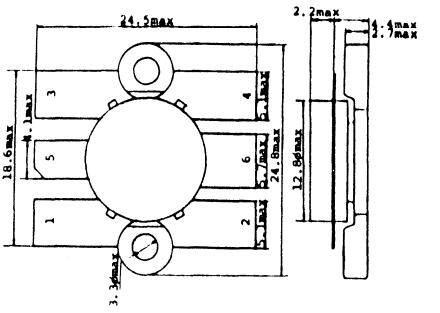
HPAK



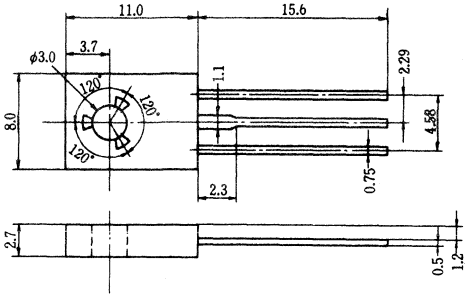


RFPAK

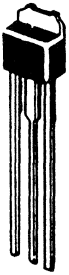


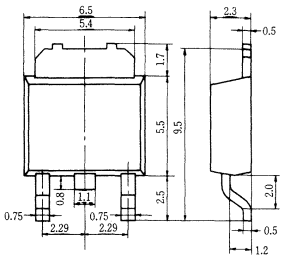


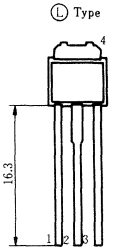
TO-126 mod



DPAK







TO-39